Application for Wind Farm Integration Complying with the Grid Code by Designing an Outer Control Strategy for the Converter.

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TRITA – EE: 2015:92
Acknowledgments

This Master of Science Thesis is the last part of my master studies in KTH and it was completed in ABB Corporate Research in Västerås. I would like to express my deepest gratitude to Hector for his guidance, help and motivation throughout these six months as well as to Georgios for his support, technical and moral. I would also like to thank Vassilios for helping me, advising me and constantly pushing me to do something more.

Without the unconditional love of my family I wouldn’t have become the person I am today.

Αλεξάνδρα
Abstract

The continuously increasing energy penetration from wind farms into the grid raises concerns regarding power quality and the stable operation of the power system. The Grid Code’s requirements give strict guidelines for a wind farm’s behaviour under faulty or abnormal operating conditions.

The primary purpose of this project is the application of a STATCOM for wind farm integration complying with the Grid Code. Towards that, an outer control strategy for the converter is designed so as to regulate the voltage at the point of common coupling by providing reactive power compensation. Thus the safe operation of the grid will be ensured since the wind farm will follow the Grid Code’s standards.

The existing Grid Code requires only a positive sequence current controller. This study attempts to investigate whether this is sufficient or not and to examine the possibility of extending the Grid Code requirements so as to incorporate a negative sequence current controller as well. The results support the latter suggestion. Also, the use of SiC devices was also considered in this project.

Key Words: Wind Farm, STATCOM, Grid Code, Positive and Negative Sequence Current Controller, Reactive Power Compensation
Sammanfattning

Den ständigt ökande penetrationen av vindenergi i elnätet väcker farhågor om elkvalitet och stabil drift av kraftsystemet. Nätkoden (Grid Code) ger strikta riktlinjer för en vindkraftsparkes beteende i felfall och under onormala driftsförhållanden.

Huvudsyftet med detta projekt är att använda en STATCOM för integration av vindkraftsparkar så att nätkoden uppfylls. I detta projekt utformas en yttre reglerstrategi för omriktaren för att reglera spänningen vid anslutningspunkten för vindkraftsparken genom att tillhandahålla reaktiv effektkompensation. Därigenom uppnås en säker drift av nätet eftersom vindkraftparken kommer att följa nätkoden.

Den befintliga nätkoden kräver endast styrning av plusföljdskomponenten av strömmen. Denna studie försöker undersöka om detta är tillräckligt samt undersöka möjligheten för att utvidga nätkoden genom att införa ett krav på styrning av negativ-sekvens ström. Resultaten stöder det sistnämnda förslaget. Även användningen av halvledarkomponenter av kiselkarbid-SiC studerades i detta projekt.
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1 INTRODUCTION

The need for renewable energy sources is increasing as our society evolves. For a sustainable environment cleaner forms of energy are essential so as to combat climate change. According to EU’s ‘20-20-20’ goals energy consumption from renewable sources must increase and energy efficiency must improve [1], [2]. At the same time, the power network should increase energy security and ensure intermittent generation at all times. Conventional power plants such as fuel oil, coal power plants etc. guarantee a safe network operation but they harm the environment. The continuous integration of renewable energy sources, however, introduces risks and challenges regarding power quality and the stability of the power system. Flexible AC Transmission Systems or FACTS are a solution towards these challenges.

1.1 Background

The current power system was designed for a single-way power transmission, from the power plants which are the centre of the network to the customers located at the edges of the network. The power contribution from the perimeters of the network or from various locations in general was not taken into account. The constantly increasing integration of renewable energy sources highlights the need for the power system to become more flexible and be able to accept all these changes. The fact that the number of installed wind turbines has been increasing rapidly raises concerns about power quality and power system stability. In order to ensure safe and stable operation as well as power quality, Grid codes are constantly being updated [2]. Every wind turbine that will be installed in the power system has to be in agreement with the corresponding country’s Grid code and should be able to fulfil the standards. Wind turbines in order to support the network, they should be able to provide with reactive power compensation. FACTS devices such as the Static Synchronous Compensator or STATCOM when they are appropriately connected to the power system they can either absorb or inject the reactive power that is needed. A STATCOM is described best as a Voltage Source Converter or VSC, without having a DC voltage source as part of the DC link. Since a VSC acts in favour of the wind farm, it is considered as a part of it, so it should comply with the Grid code as well [3].

![Figure 1.1: Simplified power system model with a STATCOM](image-url)
1.2 Aim

The aim of this master thesis is to investigate the integration of wind farms in the power network and the requirements in order to connect FACTS devices at the point of common coupling or PCC according to the Grid code. A simplified model of the system and of a STATCOM are shown in Figure 1.1. A model for the wind farm will be implemented in Simulink as well as the control of the STATCOM. Finally this control method will be evaluated.

1.3 Goal

The goals of this project are to:

- Do a literature survey on the Grid code requirements, semi-conductors, topologies, modulation strategies and control methods for the STATCOM.
- Model a wind farm and a shunt connected STATCOM on Simulink.
- Design a control strategy for the STATCOM.
- Perform simulations.
- Evaluate the existing modulation strategy and control method.

1.4 Limitations

The limitations regarding this project consider mainly the following areas:

- Only SPWM modulation strategy was implemented
- Only 2 level STATCOM was modelled
- Only Simulink was used
- Regarding the wind farm it was modelled just as a load with faults due to the fact that the focus of this project was on the control of the STATCOM.

1.5 Project Outline

The outline of this project is as follows:

- Review of wind farm technology
- Summary of Grid code requirements
- Description of STATCOM
- Review of semi-conductors
- Multilevel converters
- Modulation strategies
- STATCOM model
- Wind farm model
- Control model
- Results

1.6 Previous Work

In [2] the requirements of the Grid code regarding the integration of wind farms are presented. In [4] the flicker emission at the grid from wind turbine installations is studied.
as well as the contribution of power electronics converters in reducing voltage fluctuations. In [5], [6] the functionality of STATCOM is studied and the way it can help and support the power system. In [7], [15] a three-level converter is studied and a comparison with a two-level converter is performed.

1.7 List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FACTS</td>
<td>Flexible AC Transmission Systems</td>
</tr>
<tr>
<td>STATCOM</td>
<td>Static Synchronous Compensator</td>
</tr>
<tr>
<td>VSC</td>
<td>Voltage Source Converter</td>
</tr>
<tr>
<td>PCC</td>
<td>Point of Common Coupling</td>
</tr>
<tr>
<td>FSWT</td>
<td>Fixed Speed Wind Turbines</td>
</tr>
<tr>
<td>VSWT</td>
<td>Variable Speed Wind Turbines</td>
</tr>
<tr>
<td>IG</td>
<td>Induction Generator</td>
</tr>
<tr>
<td>SG</td>
<td>Synchronous Generator</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>DFIG</td>
<td>Double Feed Induction Generator</td>
</tr>
<tr>
<td>FRT</td>
<td>Fault Ride-Through</td>
</tr>
<tr>
<td>SVC</td>
<td>Static VAR Compensator</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>IGCT</td>
<td>Integrated Gate Commutated Thyristor</td>
</tr>
<tr>
<td>GTO</td>
<td>Gate Turn Off thyristor</td>
</tr>
<tr>
<td>MCT</td>
<td>MOS Controlled Thyristor</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MTO</td>
<td>MOS Turn Off thyristor</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon carbide</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>BIGT</td>
<td>Bi-mode Insulated gate transistor</td>
</tr>
<tr>
<td>IEGT</td>
<td>Injection Enhanced Gate Transistor</td>
</tr>
<tr>
<td>SOA</td>
<td>Safe Operation Area</td>
</tr>
<tr>
<td>NPC</td>
<td>Neutral Point diode-Clamped</td>
</tr>
<tr>
<td>SPWM</td>
<td>Sinusoidal Pulse Width Modulation</td>
</tr>
</tbody>
</table>
2 WIND ENERGY

More and more energy is coming into the power network as a result of the increasing integration of wind turbines since they are among the most common among renewable sources. One advantage of building a wind power plant over a conventional one is that it requires less time [17]. As mentioned in the introduction the European Commission’s goals suggest an increase in the energy consumption produced from renewable sources. The ultimate goal is cleaner energy, ‘green’ growth and a sustainable environment [2]. This project focuses on the integration of wind farms. In Table 2.1 and Table 2.2 some wind energy statistics are presented, according to [2], [9] and [10]:

Table 2.1: On-shore and Off-shore wind power capacity in Europe

<table>
<thead>
<tr>
<th>Year</th>
<th>On-shore installations</th>
<th>Off-shore installations</th>
<th>Cumulative On-shore Capacity</th>
<th>Cumulative Off-shore Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>2012</td>
<td>10.937 MW</td>
<td>1.166 MW</td>
<td>101.4 GW</td>
<td>5 GW</td>
</tr>
<tr>
<td>2013</td>
<td>9.592 MW</td>
<td>1.567 MW</td>
<td>110.7 GW</td>
<td>6.6 GW</td>
</tr>
<tr>
<td>2014</td>
<td>10 MW</td>
<td>1.500 MW</td>
<td>120.6 GW</td>
<td>8 GW</td>
</tr>
</tbody>
</table>

Table 2.2: Global cumulative wind power capacity

<table>
<thead>
<tr>
<th>Year</th>
<th>Cumulative Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>2012</td>
<td>283 GW</td>
</tr>
<tr>
<td>2013</td>
<td>318.1 GW</td>
</tr>
<tr>
<td>2014</td>
<td>369.5 GW</td>
</tr>
</tbody>
</table>

From Table 2.1 and according to [9], in the first half of 2014 there was a decrease in the off-shore wind power installation compare to the first half of 2013. Also, according to [9], the total capacity of all wind farms under construction in Europe is 4.9 GW.

2.1 Wind Farm Integration

- **Risks and challenges**

As the number of installed wind turbines increases, so does the concern about them affecting the power quality and the power system’s normal operation and stability [11]. Being able to predict the behavior of a wind farm is one of the main concerns due to the increasing wind power penetration into the grid [17].

As mentioned in [2], there are a few factors that can interfere with the wind power production. For the power system and the electricity market it is very important to have an accurate projection of the wind power generation. Towards that, weather and good weather knowledge play a key role. Since the wind speed varies, the wind power production varies as well. Output fluctuations can be really problematic for the grid and for the electricity market since they endanger reliable operation and have a substantial economic impact to the grid in order to match the consumption [2]. High wind speeds affect the wind power production also since for safety reasons, wind turbines are designed to shut down after a certain limit or cut-out speed (20-35 m/s).

- **Impact on the grid**

Some possible impacts the wind power penetration can have on the grid are voltage and power variation caused by the intermittent output, voltage flicker emission from the turbines, unavailability of frequency support [2], [12]. The intermittent output due to wind speed variations will have an impact on the transmission lines and the system’s inertia [13]. Thus, the weaker grids are affected the most [14]. Also, another serious issue that
affects the power system a lot is that until now wind farms will disconnect from the grid under a fault for example. Especially when the wind farm’s penetration is high that causes a lot of stability problems. As it will be explained later on, a solution to maintain power quality and system stability is transistor converters, although it increases the operation cost [14].

In order to eliminate all these problems, the grid connection rules or Grid Code are becoming tighter so as to protect the network, which will be explained in a following chapter.

- **On-shore VS off-shore**

On-shore wind farms have the benefit of smaller transmission distances compared to off-shore wind farms since they are located on land. Thus, both the investment cost and energy losses are smaller [15]. Furthermore, in off-shore wind farms the used turbines, techniques and construction also lead to increased cost [2]. Their advantage is the better wind conditions because of their geographical placement which lead to higher energy output. According to [15], [16], installation of off-shore wind farms becomes more economically efficient the bigger the project is and the more far away the park is from the shore since the capacity value can be higher there. Also the impact on the environment decreases when off-shore wind parks are further away from the shore.

- **Benefits of wind farms VS single wind turbines**

Wind speed in a wind farm can affect each turbine in a different way. So within a wind farm wind speeds will not affect the whole park in the same way, so the response time for each turbine will differ. Since not all wind turbines will be affected from potential high wind speeds, not all of them have to disconnect and thus the output fluctuations are reduced [2], [4], [17]. According to [4], the flicker effect is \(\sqrt{N}\) times lower when \(N\) smaller turbines instead of a larger one that is the same type and in the same grid. Also, their spatial distribution can affect the voltage relay protection in a positive way [17].

### 2.2 Wind Farm Technology

- **AC VS DC connection**

A very important aspect of the wind parks is designing carefully the long transmission lines between the turbines and the grid. Losses are one of the most important factors. According to [15], for distances up to 55-70 km, HVAC solution has the lowest losses. The benefits of an HVDC connection becomes apparent at distances larger than 100 km. So despite of the benefits of a DC connection, AC can still be more economically efficient especially for a medium sized wind farm. And that is taking into account the fact that AC connection will need reactive power compensation [16]. According to [15], since the biggest part of the losses are cable losses, special attention is needed when selecting the appropriate cables.

- **Wind Turbines**

- **Fixed speed wind turbines**

In fixed speed wind turbines or FSWT, the rotor speed is constant depending on their design. Factors that contribute to their design are gear ratio, generator design and grid frequency [2]. Their maximum efficiency will be at a certain wind speed. The design is simple and the cost is low. The main disadvantage is since they are directly connected to the grid, every wind speed variation will create output fluctuations that affect the grid immediately. These variations make FSWT unable to control the terminal voltage and that can be especially a problem to weak grids.
- **Variable speed wind turbines**

Variable speed wind turbines or VSWT are the most popular choice at the moment for their ability to regulate power [18]. They can adjust to the wind speed. So they have maximum or high efficiency at a large variety of wind speeds. They are connected to the grid through a converter. Since they need the use of power electronics, they are more complicated than FSWT but the power quality output is a lot better. Basically the converter separates the turbine from the grid.

- **Asynchronous VS synchronous generator’s impact on the grid**

The main difference between an induction or asynchronous generator (or IG) with a synchronous generator or SG is that the latter does not need separate excitation because it can create its own magnetic field. That can be done either by permanent magnets or electromagnets [2]. IG though in order to start their operation they need to absorb some reactive power from the network to create the magnetic field [2].

- **Double feed induction generators VS Induction generators**

Double feed induction generators or DFIG can operate at a wider range of wind speeds than IG so they can be more efficient at capturing the wind energy [11]. In case of a short circuit fault, because of their dynamic slip control and pitch control they can contribute to system’s stability. Furthermore, during short-circuit faults, DFIG show better behaviour than IG regarding stability since they can separate the output control of active and reactive power [11].

  - **Ways of turbines protecting themselves**
    - **At high wind speeds** [19]

Pitch regulated wind turbines: They require an active control system that especially at high wind speeds it will decrease the rotational speed of the turbine by varying the pitch angle of the turbine blades. In a FSWT that will lead to a decrease in the produced torque by the blades. In a VSWT that will lead to a decrease in the rotational speed of the turbine. At high wind speeds, the turbine’s blades will pitch which will slow down the turbine and protect it from damage and keep the torque constant. In case of high speeds, turbines with pitch control have increasing power up to a standard level and then it remains constant.

Stall regulated (or blade controlled) wind turbines: These turbines rely on the following control principle, when the wind speed is high, in order to protect the equipment, the rotational speed and the power production decrease. The blades are designed in a way that they perform worse at high wind speeds.

*Pitch control VS blade control*

Their basic difference is that turbines with pitch control require an active control and thus they cost more. Furthermore, they have a constant power output at high speeds whereas stall regulated turbines cannot manage that at high speeds. In general, they only show their differences at high speeds.

  - **At overcurrent** [18]

*Crowbar*

As mentioned before DFIG require a power converter to connect to the grid. This power converter can be harmed in case of an overcurrent. In order to protect the equipment there is the rotor crowbar circuit. This consists of a resistance that in case of a fault will connect the rotor phases temporarily via an Insulated Gate Bipolar Transistor or IGBT. That will result in the demagnetization of the machine.
3 GRID CODE

As the wind penetration increases in the power system, the possible consequences cannot be ignored anymore. In case of a fault, if a large wind farm shuts down that will jeopardize the safe operation of the grid. Grid codes considering that, have now adopted more strict rules regarding wind farm integration. Germany, UK, Denmark and Spain have published their own version of the Grid Code, but there are some common general principles [20].

3.1 Grid Code requirements

According to [2], the Grid Code requirements for all power generating units and for power park module focus on the following areas: frequency stability, voltage stability, robustness of power generating unit, system restoration and general system management. In this project there is a STATCOM in cooperation with the wind farm. It will be investigated how the STATCOM can support and improve the stability of the grid. According to [2], the STATCOM will contribute to the first three aforementioned areas, so these will be further analyzed below.

3.2 Grid Code and Wind Farms

- **Frequency Stability**

  These requirements are to ensure a stable frequency (in Europe 50 Hz) in the grid. Frequency ranges and expected operation times under disturbances are specified. A more detailed description of the limits and actions can be found in [2]. Outside of these limits, the wind park should protect itself. By changing the active power output, the frequency can be controlled. More specifically, in case of under or over-frequencies the wind farm can increase or decrease its active power output respectively.

- **Voltage Stability**

  These requirements specify voltage ranges and operation times. A more detailed description of the limits and actions can be found in [2]. Basically the voltage at the PCC should always be 1 p.u. The reactive power capabilities of the park will help to maintain grid stability. In case of voltage fluctuations, the wind park should be able to either absorb or inject reactive power at the PCC to ensure voltage stability. Also, the Grid Code indicates that the wind farm at specified voltages should be able to automatically disconnect. In order to perform reactive power control some measurements at the PCC are necessary. There are three possible values to be measured; voltage, reactive power and power factor. So, respectively there are three methods of performing reactive power control; voltage control method, reactive power control method and power factor control method. In case of a fault, the Grid Code indicates that the wind farm should be able to provide with the 2/3 of the needed reactive current within 10 ms. Within 60 ms it should reach its final value [2].
Robustness of the generating power unit

These requirements specify the fault ride-through or FRT capability. The FRT capability describes how a unit should behave in case of a fault.

![Figure 3.1: Low Voltage Ride-through response according to TSO](image)

Figure 3.1 shows the regulation instructed by the Grid Code that the wind farms should follow regarding FRT. A wind turbine should be able to operate normally until a voltage drop of 85% or 15% of its nominal value. It is allowed to disconnect only if the voltage drops further. FRT is one of the main challenges when designing control and protection due to the limited protection margins and strict rules in case of a fault [3].

3.3 Reactive power control capabilities

To maintain safe operation in the power system, all power plants should be able to provide with sufficient reactive power so as to ensure steady state and transient stability in case of a fault [18]. Conventional power plants (consisting of synchronous generators) traditionally can supply the grid with reactive power compensation so as to ensure voltage regulation. The limitation for that is the minimum load capability of the generating unit. It is also affected by terminal voltage limitations. Traditionally this reactive compensation is done at the point of interconnection [21].

DFIGs since they use power converters, they have dynamic voltage and reactive regulation capability. The reactive capability of a power converter is not power–limited as in synchronous generators but there are some other factors that can affect its limits such as temperature limitation, internal voltage and current limitations [21]. Their reactive power capability can be enhanced even further with an SVC or STATCOM.

In case of an IG however, since there is not a power converter they are not capable of controlling reactive power [21]. The squirrel cage IG will have many difficulties complying with the Grid Code. Their total lack of electric control forces them to disconnect from the system after a voltage drop of 10-20% [25]. There are solutions in order to improve their transient behaviour such as mechanically switched capacitors or FACTS [12].

At FSWT in order to improve the voltage control capabilities, mechanically-switched capacitor banks can be installed as well [20].

Dynamic reactive compensation, in case of a transient event can be provided almost instantaneously. Fixed capacitors or reactors can shift the power factor from lagging to
leading and vice versa and increase the system’s total reactive capability, not the dynamic. If there is insufficient reactive compensation from the generating units, dynamic reactive sources such as SVC or STATCOM may be necessary [21].
The increase of decentralized power units, especially from renewable sources as mentioned before affects the normal operation of the power system. Furthermore, as the electricity market evolves, transmission distances become longer and that stresses the grid as well. Another aspect that has an impact on the network is the fact that the system operator no longer has total control from the generation to the load as a result of unbundling the power sector. Thus power system experiences more congestion in the power lines and is need of more control techniques.

FACTS devices provide reactive compensation to the grid and when combined with control strategies can dynamically control the active and reactive power flow through the lines. So they can increase the transmission capability of the lines and the installation of new transmission lines can be avoided. Furthermore, they ensure a safe grid operation since they improve transient stability and contribute towards damping of electromechanical oscillations and overall improving the system stability. Although FACTS are expensive devices and they require more complex control compared to other existing compensation devices, for example fixed capacitors, because of the use of power electronics, they can really help optimize the usage of the electric grid [22].

FACTS devices can operate either in series with the transmission lines controlling inserted voltages or in shunt controlling inserted currents. They can be thyristor based devices like the Static VAR Compensator or SVC or IGBT based like the STATCOM.

The focus of this project is how a STATCOM can help integrate a wind farm while complying with the Grid code.

4.1 Description of STATCOM

A STATCOM is best described as VSC without a DC energy storage that is shunt connected to the grid. A VSC is DC-to-AC converter that in most cases uses IGBT technology. Figure 4.1 shows how a VSC is connected to the grid. Its basic operational principle is that it creates a desired AC voltage using the pulse width modulation method or PWM. The main function of a STATCOM is to provide controllable three-phase and without harmonics AC voltage at the PCC by providing with controllable reactive power [23]. When it is combined with an energy source, it can control the frequency as well by an additional control loop for active power exchange [26] but that increases the cost [2].

In Figure 4.2 a simplified transmission line representation is shown. Assuming that $V_i$ is the system’s AC voltage, $V_j$ is STATCOM’s AC voltage output, $\theta_{ij} = \theta_{le} - \theta_j$ is the electrical angle between nodes $i$ and $j$ and $X_L$ is the line reactance, the apparent power flow will be:

$$ S = 3 \cdot \frac{V_i \cdot V_j}{X_L} \cdot \sin \theta_{ij} - j \cdot 3 \cdot \left( \frac{V_i \cdot V_j}{X_L} \cdot \cos \theta_{ij} - \frac{V_i^2}{X_L} \right) $$

$$ = P - j \cdot Q \quad (4.1) $$

**Figure 4.1: VSC grid connection**

Where $P$ is the active power flow and $Q$ is the reactive power flow. The active power flow is affected by variations of the electric angle and the reactive power flow by the magnitude of voltage difference between $V_i$ and $V_j$. If $\theta_{ij}$ is leading then active power flows from the system to the STATCOM, if $\theta_{ij}$ is lagging then active power flows from the STATCOM to the system. If $\theta_{ij} = 0$, then the active power is zero and the reactive power is:
When $V_j > V_i$, the STATCOM provides the system with capacitive compensation since it injects current to the system. When $V_j < V_i$, the STATCOM provides the system with inductive compensation and when $V_j = V_i$, there is no reactive compensation.

\[ Q = \frac{V_i}{X_L} \cdot (V_j - V_i) \]  

(4.2)

Figure 4.2: A simplified model of the transmission line
Power semiconductor switches are basically switches that convert electrical energy. They can be categorized depending on how controllable they are. There are three main categories [24]:

1) Diodes (two-layer semiconductor devices), where both turn on and off states are dictated by the power circuit. Fast-recovery diodes with small recovery time are of interest here since they are designed to be used in high frequency circuits in parallel with controllable switches [24].

2) Thyristors (four-layer semiconductor devices), where turn on state is controlled by a control signal and turn off state by the power circuit.

3) Controllable switches, where both states are controlled by control signals, such as IGBTs, integrated gate commutated thyristors or IGCTs, injection enhanced gate thyristors or IEGTs, gate turn-off thyristors or GTOs, bipolar junction transistors or BJTs, metal oxide semiconductor field effect transistors or MOSFETs and MOS controlled thyristors or MCTs.

5.1 Thyristors

As mentioned before, thyristors are gate turn on devices but their turn off depends on the circuit. When the thyristor is at its forward-blocking region and a pulse of positive gate current is applied at the gate of the thyristor, then it can conduct like a diode and the gate pulse can be removed. Depending on the circuit, when the current tries to go negative, the thyristor will turn off and the current will go to zero. As mentioned before thyristors are used to build SVCs.

5.2 Controllable switches

For constructing a VSC, reverse-conducting switches are a requirement. Reverse-conducting switches one-direction switches with a diode connected in antiparallel. IGBTs, MOSFETs are fully controllable reverse-conducting switches or switch cells. IGCTs reverse-conducting switches are commercially available as well [27]. According to [23] among the controllable switches that are mentioned in this chapter, IGBTs and IGCTs are used the most used ones for converters for FACTS devices. Before them GTOs with antiparallel diodes were used [27]. A generic diagram of a switch cell is given in Figure 5.1.

![Figure 5.1: a.) Generic switch with diode, b) Symbolic switch cell representation](image)

- **GTO**

GTOs are four-level semiconductor devices. They are turned on by a short duration current signal with a high magnitude though and turned off by a short duration negative voltage signal. They can block negative voltages. Although GTOs are totally controllable, they cannot handle inductive turn offs which lead to over-voltages, large $\frac{dv}{dt}$, unless they are
combined with a turn off snubber circuit. This way they can reduce over-voltages but that requires the use of large capacitors [24]. They are available at high power ratings [23]. Until the early 1990s – before IGBTs- they were the main choice for high power converters [27].

- **BJT**

BJTs are current-controlled, three-layer semiconductor devices. To be at turn on state, they require continuous current supply at the base. One advantage is that they have small on state voltage, so their conduction losses are quite small. Although they have negative temperature coefficient of on state resistance, they can be connected in parallel if extra current margin is provided [24].

- **MOSFET**

MOSFETs are voltage-controlled, three-layer semiconductor devices. To be at turn on state, they require continuous gate-source voltage supply. Their on state resistance has a positive coefficient so they can be parallel-connected easily since the current can be equally distributed. This resistance increases with the device’s blocking voltage rating so only small voltage rating devices are available. However, their high on state voltage results in high conduction losses. That combined with their small switching times target their application towards lower power converters where high switching frequencies are needed [24], [27].

- **IGBT**

IGBTs are three-level, voltage-controlled semiconductor devices. They combine advantages of the aforementioned devices such as:
  - Small switch on required energy, like a MOSFET.
  - Small on state voltage, like a BJT. For example a 2-3 V for a 1kV device.
  - They can block negative voltages, like a GTO.

They have short turn on and turn off times – on the order of 1 μs- and they are available for large current ratings (up to 1.2 kA) and medium voltage ratings (up to 1.7 kV) [23], [24]. In the future is expected for IGBTs to be available for high voltage ratings as well (up to 2-3 kV) [24].

IGBTs are unidirectional switches. In order for an IGBT to conduct after a turn on signal, current has to flow from the collector (C) to the emitter (E) as shown in Figure 5.2.

![IGBT symbol](image.png)

**Figure 5.2: IGBT symbol**
• IGCT

IGCT is a current-controlled device that was introduced by ABB [28], [29]. It consists of silicon wafer. They are structured like GTOs - they turn off like transistors but conduct like thyristors [29]. They have smaller on state voltage than IGBTs so they have lower conduction losses. They have negative temperature coefficient and can be switched faster than GTOs [27]. These characteristics make them cost effective [29].

IGCTs can handle higher overvoltages than GTOs so they do not require a turn off snubber circuit in every application. They can safely handle currents up to 3.6 kA but that implies more effort to control them compared to IGBTs. Because IGCTs are thyristor-based devices, they require higher turn on and turn off energy, so they cannot be operated at very high frequencies as transistors can. They can operate up to 10 kHz so as to regulate switching losses. Another disadvantage compared to the IGBT, is that because of the thyristors, the transition from on to off state is not stable and it results in overcurrents [28]. A protective circuit or clamp circuit is therefore used to limit these on state overcurrents [29] and protect the freewheeling diodes [30].

Overall, their efficient cooling, low losses make and their ability to handle very high power make them a good choice for very large power converters that will operate at lower frequencies [28].

In Figure 5.3 the basic topologies for an IGBT and an IGCT 3-phase inverter are presented.

![IGBT Inverter](image)

![IGCT Inverter](image)

**Figure 5.3: Basic IGBT and IGCT inverter topologies**

• MCT

MCT is a voltage-controlled semiconductor device. It consists of two MOSFETS of opposite conductivity, the ON-FET and the OFF-FET. Like the MOSFET and the IGBT, MCT has the benefit of small switch on required energy and lower on state losses compared to an IGBT or a MOSFET because of its reduced cell size. Compared to a GTO, it has faster switching times. Also it is designed for high power converters and is capable of handling large currents [24].
- **MTO**

MTOs are current-controlled turn on devices, like a thyristor and voltage-controlled turn off devices having a MOS structure. Compared to a GTO, a MTO has reduced losses, higher switching speed and fewer components which makes its application easier [33].

- **BIGT**

The BIGT concept introduces a single chip reverse conducting IGBT instead of a standard IGBT/diode two chip. Both the standard IGBT and BIGT are based on Soft Punch Through buffer design. Thus it is difficult to control the bipolar gain especially for higher voltage ratings. There are some requirements that in order to be fulfilled, the gain must be adjust. These are:

  - Reverse Blocking Safe Operation Area (RBSOA)
  - Short circuit Safe Operation Area (SOA)
  - Losses
  - Leakage Current

The most important design characteristic of the BIGT is the introduction of anode shorts. That will help towards diode conduction and improvement of overall device functionality. The main advantages of BIGT over IGBT are listed below:

  - Improved thermal capability at higher temperatures.
  - Reduced leakage current.
  - Soft performance under all operating conditions (no abrupt drops).
  - Better turn off performance.
  - Improved short-circuit SOA capability.

However there are some challenges when designing BIGTs such as the snap-back effect in the I-V characteristics [35].

- **IEGT**

IEGTs are fully controllable semiconductor devices with high efficiency. They are rated for high power use. Their characteristic is low in state resistance and they realize low saturation voltage by injection enhanced effect [34].
Table 5.1: Comparison of basic semi-conductor characteristics

<table>
<thead>
<tr>
<th>Control Signal</th>
<th>On state voltage/Conduction losses</th>
<th>Switching time/ Switching losses</th>
<th>Power rating</th>
<th>Switching frequency</th>
<th>Turn-off overvoltages</th>
<th>Turn-on overcurrents</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTO</td>
<td>-</td>
<td>High</td>
<td>Fast (esp. turn on)/ low losses</td>
<td>High</td>
<td>Small (higher than thyristor)</td>
<td>Needs snubber</td>
</tr>
<tr>
<td>BJT</td>
<td>Current</td>
<td>Small</td>
<td>Not fast/ high losses</td>
<td>Low-medium</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>MOSFET</td>
<td>Voltage</td>
<td>High (higher than MCT)</td>
<td>Fast (faster than BJT, more slow than GTO)/ lowest turn-off losses of all</td>
<td>Low-medium</td>
<td>Very high (the highest)</td>
<td></td>
</tr>
<tr>
<td>IGBT</td>
<td>Voltage</td>
<td>Small (smaller than MOSFET)</td>
<td>Fast (faster than BJT)</td>
<td>Medium-high</td>
<td>Quite high (higher than GTO)</td>
<td></td>
</tr>
<tr>
<td>IGCT</td>
<td>Current</td>
<td>Small (smaller than GTO)</td>
<td>Quite fast (faster than GTO)/ losses not small</td>
<td>High</td>
<td>Smaller than IGBT</td>
<td>Better than GTO, snubber in some cases</td>
</tr>
<tr>
<td>MCT</td>
<td>Voltage</td>
<td>Small</td>
<td>Not so fast (faster than GTO)</td>
<td>High</td>
<td>Snubber in some cases</td>
<td>Snubber in some cases</td>
</tr>
<tr>
<td>Thyristor</td>
<td>-</td>
<td>Small</td>
<td>Not so fast</td>
<td>High (the highest)</td>
<td>Small (the smallest)</td>
<td>limited</td>
</tr>
</tbody>
</table>

Si versus SiC switches

Over the years switches based on wide bandgap materials (such as silicon carbide or SiC and gallium nitride or GaN) have shown really good overall performance. The comparison between silicon or Si and SiC switches is of interest here and is presented in Table 5.2 [31], [32].

Table 5.2: Si versus SiC switches

<table>
<thead>
<tr>
<th>Requirements</th>
<th>SiC VS Si switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction losses</td>
<td>Lower</td>
</tr>
<tr>
<td>Thermal capabilities</td>
<td>Better</td>
</tr>
<tr>
<td>Cost</td>
<td>Lower</td>
</tr>
<tr>
<td>Turn on losses</td>
<td>Lower</td>
</tr>
<tr>
<td>Frequency limits</td>
<td>Higher</td>
</tr>
</tbody>
</table>

Regarding their thermal capabilities, SiC switches have higher junction temperatures. Theoretically, they can go up to $500^\circ C$. Normally they can go up to $200^\circ C$, whereas Si
switches have junction temperatures at $150 - 175^\circ C$. These limits can increase but that will increase the losses in the Si devices [32].

A very important improvement that SiC switches offer is reduced turn on losses. As a result, for the same desired output, the converter’s efficiency is higher. Or alternatively, for the same semiconductor losses, the power output is higher. Also, for the same semiconductor losses, SiC switches can be operated in higher switching frequencies. Thus the size of the output filter can be reduced as well as its cost [31].

5.3 Power Dissipation in Controllable Switches (Losses)

The power losses on a semi-conductor belong in two categories: conduction and switching losses. According to [24], the following formulas can be used (without considering a parallel diode with the semi-conductor):

For calculating the average conduction (or on-state) dissipated power:

$$P_{on} = (V_{on} \cdot I_o + R_{on} \cdot I_o^2) \cdot t_{on} \cdot \frac{1}{T_s}$$  \hspace{1cm} (5. 1)

For calculating the switching power losses:

$$P_{sw} = \frac{1}{2} \cdot V_d \cdot I_o \cdot t_{on} \cdot \frac{1}{T_s} \cdot \left[ t_{c(on)} + t_{c(off)} \right]$$  \hspace{1cm} (5. 2)

Where:
- $V_{on}$ is the on-state voltage
- $R_{on}$ is the slope resistance
- $V_d$ is the blocking state voltage
- $I_o$ is the conducting current
- $t_{c(on)}, t_{c(off)}$ are the crossover intervals
- $T_s$ is the switching period

It is interesting to mention, that if the semi-conductor is a MOSFET then the on-state voltage is almost zero. Thus, the conduction losses are smaller than those in an IGBT. This is very important especially in the case of a chain-link STATCOM. There, the switching frequency can be 3 or 5 times the fundamental frequency which is not a lot. So, almost all the losses are conduction losses and then advantages of using MOSFETS are clear.
In this section a brief comparison between STATCOM and SVC is given. Their main difference is that STATCOM is a VSC. SVC is a thyristor based device and STATCOM is an IGBT based one. The use of the latter has many advantages over the SVC. Some of them are described here below:

- **STATCOM**, due to its VSC configuration can provide with very fast control because of the IGBTs. Its response time is a lot faster than for the SVC, since the thyristors do not allow control over their turn off state [23].

- It is capable of generating the needed reactive power, so it does not require any additional capacitance or inductance. Hence it is more compact than an SVC [22], [23]. That, from the installation point of view, is very convenient. Since it requires less physical space it is better for locations where land is expensive and also if is needed to be relocated, it is more suitable [26]. Also, in many cases STATCOM is in a container.

- As far as losses are concerned, at zero reactive output both SVC and STATCOM have low losses. As the reactive output increases so are the losses. The controllable switches in the STATCOM however result in higher losses compared to the thyristors in the SVC [26].

- Within their linear capabilities, both devices have similar behavior. Outside though of their limits, there are differences. The V-I and V-Q characteristics can be found in [26]. One very important feature of the STATCOM that can be seen in its V-I characteristic is that when it reaches its limits it is still able to provide reactive current with maximum capability even if the system voltage drops to 0.2 p.u., which contributes for the FRT capability [25]. That basically means that the STATCOM output is independent of the system voltage which is not the case for the SVC. When the SVC reaches its limits, it can be represented as a fixed admittance that decreases linearly with the system voltage as it drops [22]. From the V-Q characteristics for each device, it is clear that at low voltages, STATCOM decreases its reactive output capability linearly with the voltage drop while SVC’s reactive output capability decreases with the square of the system’s voltage drop. The reactive output for STATCOM can be described by [22]:

\[ Q_{ST} = I_{max} \cdot U \]  

Equation (6.1) applies for the SVC as well, but since at its limits it is represented as an admittance, \( B \), it is [22]:

\[ Q_{SVC} = I_{max} \cdot U = B \cdot U^2 \]  

So at low voltage levels, STATCOM is more robust and effective since it can provide higher reactive power than the SVC [26], [22]. That also improves the system’s transient stability by increasing the stability margin [26].

- If a STATCOM is combined with an energy source, it can exchange active power as well. SVC cannot contribute towards active compensation [26].

Overall, STATCOM enhances the system's transient stability more as well as the FRT capability [25].
VSCs for high power applications are expected to handle high voltage and high power ratings. A single switch cannot handle high voltages and high powers. The goal is to surpass these limitations and increase the ratings. Towards that, there are two basic configurations: Multimodule VSC systems and multilevel VSC systems.

7.1 Multimodule VSC systems

A power semiconductor combined with a diode form a switch as shown in Figure 5.1. In order to overcome the voltage/ power limitations mentioned before, these switches can be connected in series or in parallel so as to form a module for the VSC. These modules then can be connected in parallel, so as to form a multimodule VSC that will have an increased power rating. More precisely, for every module that will be parallelized, the power will be increased so many times. Since every module is the same with each other and that applies for the needed transformers as well, the VSC has modularity. Modularity provides with many advantages the system such as reduced manufacturing cost and easier maintenance. It is also very important for the converter’s availability.

When connecting switches in series it is important that they can handle the voltage requirements. However according to [27] there are practical limitations that allow only a limited number of series-connected switches in a two-level module, such as unequal voltage distribution during turn-off period, strict requirements about simultaneous-gating for the semiconductors and unacceptable levels of harmonic distortion. Thus multilevel systems are superior.

7.1.1 2 level converter

Combining two switches in series creates a half-bridge configuration as shown in Figure 7.1. This is a single-phase, 2-level converter. It is called a two level converter because the phase-to-neutral AC output voltage has two discrete peak values [37].

Combining two half-bridges in parallel creates a full-bridge or H-bridge configuration as shown in Figure 7.2, which is referred to as a cell. This is the single-phase, 2-level VSC. Only one switch of each of the two legs should be conducting at all times. Again, the phase-to-neutral AC output voltage will have two discrete peak values.

Combining three half-bridges in parallel creates a three-phase, full-bridge configuration as shown in Figure 7.3. This is the three-phase, 2-level VSC. Only one switch of each of the three legs (three switches in total) should be conducting at all times. There are 8 conducting states where 6 are non-zero. Again, the phase output voltage will have two discrete peak values. The output line-to-line voltages will have three discrete values [37]. Three phase converters cover from low power to medium to high power applications.
7.2 2 level versus multilevel converters

Their main advantage over 2-level converters is the fact that the synthesized voltages of multilevel converters containing lower levels of harmonic distortion without decreasing the converter’s output [36]. Thus they require smaller filters. They can also reduce the overvoltage switch stress. Multilevel converters can operate at the fundamental switching frequency as well as at high switching frequency, although at lower switching frequencies, the losses are smaller as well.

The main disadvantage of multilevel converters is the use of more semiconductor switches and the fact that the system’s control becomes more complex.

7.3 Multilevel VSC systems

The basic aim of a multilevel converter is to achieve high power by synthesizing a staircase voltage using a series of semiconducting switches with lower DC voltages. Multilevel converters are increasingly being used for high power and medium voltage energy control. They are used with renewable sources since they allow their connection to the grid without voltage fluctuation problems [37]. With the 3-level converter, the term multilevel converter initiated.

7.3.1 Multilevel VSC topologies

The basic multilevel converter topologies are:

- Diode-clamped multilevel VSC / Neutral-point- clamped VSC
- Flying-capacitor (or capacitor-clamped) multilevel VSC
- Cascaded H-bridge based multilevel VSC / Chain link STATCOM

7.3.1.1 Diode-clamped (neutral clamped)

In a three-phase diode-clamped converter, each phase shares a common DC bus. According to the desired output voltage level, this DC bus is divided with capacitors so the voltage level is the same across each one of them and equal i.e. to $V_{dc}/m$. For an $m$-level phase output voltage (the line output voltage will be $(2 \cdot m - 1)$), $m-1$ capacitors are needed. The leg for each phase has $m-1$ complementary switch pairs, so $2 \cdot (m - 1)$ switches in total per phase. At any given time $m-1$ adjacent and in series
switches must be on. The clamping diodes for each switch pair limit the voltage stress to \( V_{dc}/2 \).

The advantages of this configuration is that every phase shares a common DC bus which reduces a lot the number of needed capacitors. Furthermore, the common DC bus facilitates the back-to-back connection. These capacitors can be precharged as a group. Lastly, at the fundamental switching frequency, the efficiency of this configuration is high.

The main disadvantage of the diode-clamped converter is the fact that a large number of clamping diodes is needed. As mentioned before, these diodes limit the voltage stress at each switch at \( V_{dc}/2 \). Assuming that all diodes have the same voltage rating, as the output voltage level increases, so does the number of the diodes that need to be connected in series to handle this voltage level. So, for each phase \((m - 1) \cdot (m - 2)\) diodes are required. Thus, the output voltage level is limited because of the increased number of components and complexity of the system. Realistically, this topology can be used for up to a five-level converter. Another disadvantage is that the losses are not equally distributed to the semiconductors, which limits the switching frequency range [38]. Furthermore, for this topology as well, the real power exchange is difficult [27], [37]. One of the main concerns about this topology though is the balance of the voltages at the DC side capacitors. With different control strategies and using the output voltage redundancy that the topology offers the problem can be mitigated [38].

⇒ **Neutral-Point-Clamped Converters**

The Neutral Point diode-clamped or NPC converter, is widely used for high power applications and offers high reliability and availability. With an NPC, the number of series-connected switches is reduced. For a three-level application, each phase leg consists of two complementary switching pairs, so four switches in total and also two clamping diodes. At the DC side the capacitor is divided then in two equal voltage levels with the neutral point being in the middle. That midpoint is connected to the converter through the clamping diodes so as to limit the voltage across the switch to the voltage level corresponding to one capacitor at the DC bus [27].

### 7.3.1.2 Flying capacitors (capacitor-clamped)

The topology of a flying capacitors or capacitor-clamped multilevel converter is similar to the diode-clamped one but instead of the clamping diodes in each phase leg there are capacitors. Thus it requires a large number of large capacitors which can reduce the topology’s reliability.

The DC side consists of capacitors with different voltage level for each one. For an \( m \)-level desired phase output voltage (the line output voltage will be \((2 \cdot m - 1))\), \( m-1 \) capacitors are needed, like in the diode-clamped configuration.

For each phase leg, assuming that all capacitors have the same voltage rating, as the output voltage level increases, so does the number of capacitors that need to be connected in series to handle this voltage level. So, for each phase \((m - 1) \cdot (m - 2)\) \(\frac{2}{2}\) capacitors are required [37]. Unlike the diode-clamped topology, the switches that are on in each phase leg do not have to be in a continuous row.

The inner (phase) voltage level redundancy that this configuration offers is an advantage. That is, there are more than one switching combinations for an output voltage level. Like with the diode-clamped topology, the common DC bus is an advantage. Another
advantage is that both active and reactive power flow can be controlled. Furthermore, the capacitors increase the FRT capability of the converter.

There are some disadvantages though that make this topology not so widely used in practice. The main challenge of the topology is to regulate the capacitors’ voltage. Moreover, the large number of used capacitors, increase the topology’s cost [37].

7.3.1.3 Cascaded H-bridge converters with separate DC source or Chain-link

A cascaded H-bridge based VSC converter consists of H-bridge modules connected in series with separate DC sources. This way their AC output voltages can be summed up. The level, $m$, of the output voltage is equal to:

$$m = 2 \cdot s + 1$$

(7.1)

Where $s$ is the total number of separate DC sources or cells connected in series. The bigger the $m$, the closest at a sinusoidal wave the output AC voltage will be. Before connecting to the grid, there is an inductor for each phase ‘leg’. The output waveform contains only odd harmonics. By changing the conducting angles of the semi-conductors the 5,7,11,13th harmonics can be eliminated.

This topology is more suited for applications where reactive power exchange is needed, like STATCOM. In order to handle real power exchange, the DC-bus voltage of each module must be supplied and controlled [27].

An advantage of this topology is the fact that the available levels for the output voltage are more than the number of separate DC sources ($m > s$). Furthermore, this configuration is characterized with modularity since it consists of series-connected identical H-bridges. One the main advantages of this topology regarding a chain link failure, is a built-in feature just by adding an extra cell into the each phase chain. In a case of a failure, the faulty cell operates as a short circuit until its maintenance. It is well understood that this is feasible because of the topology’s modularity [39].

The disadvantage of the topology in a chain-link STATCOM application is the need for a large number of DC capacitors for individual energy storage at each cell [27], [37]. It is also very important to mention the negative sequence present during unbalance conditions will require extra capacitance on each cell.

8 MODULATION STRATEGIES

The AC output voltage of a converter in a STATCOM application should follow a desired, sinusoidal waveform. In reality though, the output waveform has steps. By using a modulating technique to control the switching of the semiconductor devices, the goal is that the output waveform will follow the desired one.

8.1 Single phase converters (2 level)

For the two 2-level single phase semiconductor configurations, the proposed modulation strategies are given below.

8.1.1 Half bridge based converters

As mentioned before, in a half bridge, at all times only one of the two switches should be on. If both are at the on state, then a short circuit is created at the DC bus. A modulation strategy should make sure that this will not happen.

- Carrier-based PWM
This modulation technique manages to control the switching of the two switches by comparing the desired AC output waveform with a triangular waveform. The former is the modulating signal, \( v_c \), and the latter is the carrier signal, \( v_A \). When \( v_c > v_A \), then the upper switch is conducting. When \( v_c < v_A \), then the lower switch is conducting.

**Sinusoidal PWM or SPWM**

If the modulating signal is a sinusoidal waveform with frequency \( f_c \) and amplitude \( \tilde{v}_c \) and the carrier signal is at frequency \( f_A \) and has amplitude \( \tilde{v}_A \), then this carrier PWM is called sinusoidal PWM or SPWM. The AC output voltage is a sinusoidal waveform with harmonics.

The modulation index is:

\[
m_a = \frac{\tilde{v}_c}{\tilde{v}_A}
\]  
(8. 1)

If \( m_a \leq 1 \), then the modulation is within the linear region. If \( m_a > 1 \), then it leads to overmodulation.

The normalized carrier frequency is:

\[
m_f = \frac{f_A}{f_c}
\]  
(8. 2)

If \( m_f \) is an odd number, then the harmonics appear at the normalized frequency \( f_h \), around \( m_f \) and its multiples. So it is:

\[
h = l \cdot m_f \pm k \text{ where } \begin{cases} k = 2, 4, 6, \ldots & \text{if } l = 1, 3, 5, \ldots \\ k = 1, 3, 5, \ldots & \text{if } l = 2, 4, 6, \ldots \end{cases}
\]  
(8. 3)

The amplitude of the fundamental component is:

\[
\tilde{v}_{o1} = \frac{V_i}{2} \cdot m_a
\]  
(8. 4)

where \( V_i \) is the DC link voltage. It is obvious that in the linear region, the maximum amplitude of the fundamental component is \( \frac{V_i}{2} \).

The amplitude of the AC voltage output harmonics is a function of \( m_a \) and it is independent of \( m_f \) if \( m_f > 9 \).

For rather small values of \( m_f \) (\( m_f < 21 \), \( m_f \) should be an integer, so that \( v_c \) and \( v_A \) are synchronized. Otherwise, subharmonics will appear. If \( m_f > 21 \), these subharmonics are negligible.

There are also harmonics in the DC link current. These appear at the normalized frequency \( f_p \), around \( m_f \) and its multiples. So it is:

\[
p = l \cdot m_f \pm k \pm 1 \text{ where } \begin{cases} k = 2, 4, 6, \ldots & \text{if } l = 1, 3, 5, \ldots \\ k = 1, 3, 5, \ldots & \text{if } l = 2, 4, 6, \ldots \end{cases}
\]  
(8. 5)

One very important feature of this modulation technique regarding the harmonics is that their amplitude and the frequency they appear in are very well defined, so filtering is easier [37].

**Overmodulation**

As mentioned before, the overmodulation region is for \( m_a > 1 \). Although, the fundamental component’s amplitude can be higher, overmodulation leads to low-order harmonics.
If \( m_o \) becomes a lot bigger \( (m_o > 3.24) \), then the output AC voltage is basically a square which is another modulating technique.

#### Square Wave Operation

Here, both switches should be on for half of the switching cycle, so that the output AC voltage is a square waveform. Only odd harmonics appear. The amplitude of the fundamental component is:

\[
\hat{V}_{o1} = \frac{4}{\pi} \frac{V_i}{2}
\]  
(8. 6)

The harmonics’ amplitudes are:

\[
\hat{V}_{oh} = \frac{\hat{V}_{o1}}{h}, \text{where } h = 3, 5, 7, ...
\]  
(8. 7)

#### Selective Harmonic Elimination

The concept of this strategy is to keep the AC output voltage sinusoidal by adjusting the fundamental component and eliminating a number of harmonics. This can be done by calculating the exact turn on/off of the semiconductor cells. The AC output voltage has odd half and quarter wave symmetry, so there are no even harmonics. To eliminate \( N - 1 \) number of harmonics, the AC output should be chopped \( N \) times per half cycle to adjust the fundamental component.

In order to eliminate an even number of harmonics and adjust the fundamental component, the following general expressions are used respectively:

\[
- \sum_{k=1}^{N} (-1)^k \cdot \cos(n \cdot a_k) = \frac{1}{2}, \text{where } n = 3, 5, \ldots \text{the order of the harmonic}
\]  
(8. 8)

\[
- \sum_{k=1}^{N} (-1)^k \cdot \cos(a_k) = \frac{2 + \pi \cdot \hat{V}_{o1}}{4}
\]  
(8. 9)

The angles should satisfy the following requirement:

\[
a_1 < a_2 < \ldots < a_N < \pi / 2
\]  
(8. 10)

In [37], there are plots that specify these angles.

Similarly, to eliminate an odd number of harmonics and adjust the fundamental component, the following general expressions are used respectively:

\[
- \sum_{k=1}^{N} (-1)^k \cdot \cos(n \cdot a_k) = \frac{1}{2}, \text{where } n = 3, 5, \ldots, 2N - 1 \text{ the order of the harmonic}
\]  
(8. 11)

\[
- \sum_{k=1}^{N} (-1)^k \cdot \cos(a_k) = \frac{2 - \pi \cdot \hat{V}_{o1}}{4}
\]  
(8. 12)

The angles should satisfy the following requirement:
In [37], there are plots that specify these angles.

### 8.1.2 Full bridge (or H-bridge) based converters

As mentioned before, in a single-phase full-bridge, at all times either the upper or the lower switch of each leg should be on the on state. Otherwise a short circuit is created at the DC bus. A modulation strategy should make sure that this will not happen. As mentioned before, with the half bridge configuration, the maximum AC voltage output amplitude is \( \frac{V}{2} \). With this configuration, the maximum amplitude can be equal to the DC link voltage (\( v_i \)).

#### Bipolar PWM

A single sinusoidal wave is used here. There are two discrete states. One of the two cells of each leg must conduct at all times. More specifically there are two combinations for the on state:

\[
(S_1^+ \text{ and } S_2^-) \text{ or } (S_1^- \text{ and } S_2^+)\]

This means that the output AC line-to-line voltage will have two discrete peaks, \( v_i \) and \(-v_i\).

The maximum amplitude can be equal to the DC link voltage (\( v_i \)). The fundamental component (line-to-line voltage) of the AC voltage output, for the linear modulating region, is:

\[
\tilde{V}_{o1} = \tilde{V}_{ab1} = V_i \cdot m_a
\]  

In the overmodulating region, it is:

\[
V_i < \tilde{V}_{o1} = \tilde{V}_{ab1} < \frac{4}{\pi} \cdot V_i
\]

#### Unipolar PWM

Two sinusoidal modulating signals are used here to generate two output voltages, \( V_{aN} \) and \( V_{bN} \). There are four conducting states, so the output AC line-to-line voltage will have three discrete peaks, \( v_i \), \(-v_i\) and \(0\). The two signals are \( v_c \) and \(-v_c\), so the two output phase-to-neutral voltages from each leg will be:

\[
V_{aN} = -V_{bN}
\]

The fundamental component of the line-to-line output AC voltage will be:

\[
V_{o1} = V_{aN1} - V_{bN1} = 2 \cdot V_{aN1}
\]

Because of (8.16), (8.17) will not contain even harmonics.

And like with the bipolar PWM:

\[
\tilde{V}_{o1} = \tilde{V}_{ab1} = V_i \cdot m_a = 2 \cdot \tilde{V}_{aN1}
\]

If \( m_f \) is an even number, then the harmonics appear at the normalized odd frequency \( f_h \), around twice the carrier frequency \( m_f \) and its multiples. So it is:

\[
h = l \cdot m_f \pm k \text{ where } k = 1, 3, 5, \ldots \text{ if } l = 2, 4, 6, \ldots
\]

The harmonics in the DC link current appear at the normalized frequency \( f_p \), around twice the carrier frequency \( m_f \) and its multiples. So it is:

\[
p = l \cdot m_f \pm k \pm 1 \text{ where } k = 1, 3, 5, \ldots \text{ if } l = 2, 4, 6, \ldots
\]
This feature is an advantage of the unipolar PWM since it allows for smaller filters with the same switching frequency compared to the bipolar PWM [37].

Selective Harmonic Elimination

This technique is applied in a per line way for a full bridge VSI. The output AC voltage, like with the half-bridge SHE, has odd half and quarter wave symmetry. So there are no even harmonics. Here as well, the AC output voltage is kept sinusoidal by adjusting the fundamental component and eliminating a number of harmonics. This can be done by calculating the exact turn on/off of the semiconductor cells. To eliminate \( N - 1 \) number of harmonics, the AC output should be chopped \( N \) times per half cycle to adjust the fundamental component (so \( N \) pulses per half cycle). To eliminate an odd number of harmonics and adjust the fundamental component, the following general expressions are used respectively:

\[
- \sum_{k=1}^{N} (-1)^k \cdot \cos(n \cdot a_k) = 0, \text{where } n = 3, 5, \ldots, 2N - 1 \text{ the order of the harmonic}
\]

\[
- \sum_{k=1}^{N} (-1)^k \cdot \cos(a_k) = \frac{\pi}{4} \cdot \left( \frac{\bar{V}_{o1}}{\bar{V}_t} \right)
\]

The angles should satisfy the following requirement:

\[
a_1 < a_2 < \ldots < a_N < \pi/2
\]

In [37], there are plots that specify these angles.

Voltage cancellation

A special case is when only the fundamental component is controlled. Two phase-switched square wave signals are used, with the phase angle being \( 2 \cdot a_1 \). The amplitude then of the fundamental component and the harmonics will be:

\[
\bar{V}_{oh} = \frac{4}{\pi} \cdot V_t \cdot \frac{(-1)^{h-1/2}}{h} \cdot \cos(ha_1), \text{where } h = 1, 3, 5, \ldots
\]

For \( a_1 = 0 \), square wave operation is achieved.

8.2 Three phase converters

For the three phase semiconductor configurations, the proposed modulation strategies are given below. Firstly the 2-level VSC modulation techniques are analysed and then for multilevel VSCs.

8.2.1 Two level converters

The configuration as mentioned before, is the three-phase full bridge VSC.

Sinusoidal PWM

It requires three modulation signals with 120° phase difference and one carrier signal with \( m_f \) being an odd number. So, all three phase AC output voltages will have the same amplitude and 120° phase difference. The modulation signal for each phase is compared with the triangular carrier waveform. When the modulation signal is higher than the carrier, then the upper IGBT of the bridge phase leg is ON and the lower one is OFF. When is lower, then the upper IGBT is OFF and the lower IGBT is ON. In Figure 8.1 is shown in which order the IGBTs are conducting.
Figure 8.1: Conducting order of IGBTs

Regarding the harmonics, those that are multiples of 3 have the same amplitude and phase at all three phases. Thus, the resulting line-to-line voltage will not contain these harmonics. For odd multiples of $m_f$, the harmonics are centered around $m_f$ and its multiples and not on multiples of 3:

$$h = l \cdot m_f \pm k \quad \text{where} \quad \begin{cases} l = 1, 3, 5, \ldots \text{if } k = 2, 4, 6, \ldots \quad (8.25) \\ l = 2, 4, 6, \ldots \text{if } k = 1, 5, 7, \ldots \end{cases}$$

The harmonics in the DC link current appear at the normalized frequency $f_p$, around twice the carrier frequency $m_f$ and its multiples. So it is:

$$p = l \cdot m_f \pm k \pm 1 \quad \text{where} \quad \begin{cases} l = 1, 3, 5, \ldots \text{if } k = 2, 4, 6, \ldots \quad (8.26) \\ l = 0, 2, 4, \ldots \text{if } k = 1, 5, 7, \ldots \end{cases}$$

The factor $(l \cdot m_f \pm k)$ should not be a multiple of 3.

The maximum amplitude is equal to $\sqrt{\frac{3}{2}} V_i$. The fundamental component (line-to-line voltage) of the AC voltage output, for the linear modulating region, is:

$$\tilde{V}_{o1} = \tilde{V}_{ab1} = \sqrt{\frac{3}{2}} V_i \cdot m_a \quad (8.27)$$

In the overmodulating region, it is:

$$\frac{\sqrt{3}}{2} V_i < \tilde{V}_{o1} = \tilde{V}_{ab1} = \tilde{V}_{bc1} = \tilde{V}_{ca1} < \frac{4}{\pi} \cdot \sqrt{\frac{3}{2}} V_i \quad (8.28)$$

- **Square Wave Operation**

If $m_a$ becomes high, that leads to the square wave modulating technique. The switch cells are on for 180° (half switch cycle), like with the single phase half bridge. The amplitude of the fundamental component is:

$$\tilde{V}_{o1} = \tilde{V}_{ab1} = \frac{4}{\pi} \cdot \frac{\sqrt{3}}{2} V_i \quad (8.29)$$

Thus, the only way to control the AC (or load) voltage is by the DC link voltage, $V_i$.

The amplitudes of the harmonics are:

$$\tilde{V}_{ab1} = \frac{1}{h} \cdot \frac{4}{\pi} \cdot \frac{\sqrt{3}}{2} V_i \text{, where } h = 6k \pm 1 \text{ for } k = 1, 2, 3, \ldots \quad (8.30)$$

- **Sinusoidal PWM with zero sequence signal injection**

By adding a zero sequence signal to the regular modulation signals before they are compared to the carrier signal, the linear region is expanded:

$$0 < m_a \leq \frac{2}{\sqrt{3}} \quad (8.31)$$
This can be achieved because the zero sequence signal can reduce the amplitude of the modulating signals and thus utilize the DC link voltage better.

The amplitude of the AC phase output voltage is $\frac{V_l}{\sqrt{2}}$, so for the line-to-line voltage is $V_l$. For the fundamental component it is:

$$\tilde{V}_{a1} = \tilde{V}_{ab1} = \frac{3}{2} \cdot V_l \cdot m_a$$

8. Selective Harmonic Elimination

The same technique as for in single phase converters can be applied here. Again, there are no even harmonics. Furthermore all harmonics that are odd multiples of 3 are missing as well.

8. Space Vector based modulation

With this method, the three-phase variables are represented from the abc frame to the $\alpha\beta$ frame. For example, the vector with the line-to-line voltages can be represented in the $\alpha\beta$ frame with a complex vector. This vector will contain a real part ($\alpha$) and an imaginary part ($\beta$).

As mentioned before, there are 8 conducting states (6 are non-zero and 2 are zero) and three discrete levels for the AC line-to-line output voltage: $V_l, 0$ and $-V_l$. So there will be six non-zero complex line voltage vectors and two zero line voltage vectors, 8 in total. The six non-zero voltage vectors will divide the $\alpha\beta$ plane in 6 parts or switching state vectors (SSVs).

The idea is to approximate the modulating vector ($\overrightarrow{v}_m$) with the line voltage vectors ($\overrightarrow{v}_l$). There are many possible combinations to do that. However according to [37], [40] when the used SSVs are not adjacent, then higher THD is produced as well as higher switching losses. Thus the proposed way is to synthesize the modulating vector by the PWM of two adjacent SSVs and a zero voltage vector.

The advantage of SVM over SPWM is the fact that when the former, the maximum amplitude for the fundamental component is $\frac{\sqrt{3} V_l}{2}$.

8.2.2 Multilevel converters

In multilevel converters, the modulation strategies can be classified according to the switching frequency: fundamental switching frequency and high switching frequency PWM [37], [41]. Regarding switching at the fundamental frequency, is not for a STATCOM application but to give a more complete understanding about the PWM capabilities. Basically switching at the fundamental frequency, leads in a squared-wave AC output and this should be avoided in a STATCOM application where a sinusoidal AC output is needed. Otherwise, the THD will be really big and large filters should be used.

8.2.2.1 Fundamental switching frequency

At the fundamental switching frequency, the semiconductor switches conduct once or twice per cycle of the output voltage with modulation methods mentioned below. That way, in a multilevel converter, a staircase voltage is created at the converter’s AC output.

- Space Vector Control or (SVC)

This method is very simple and attractive for a high number of levels. The higher number of levels, the higher the density of the produced vectors [41]. The main idea of SVC is to minimize the error among a quantity and its reference value that will eventually deliver to
the load. The high density of these vectors leads to small errors. Also, as the number of
the levels decrease, the ripple at the load current increases since the error increases.

- Selective Harmonic Elimination

The selective harmonic elimination for the fundamental switching frequency can also be
called fundamental switching frequency method. By appropriately choosing the conducting
angles of the switches, lower order harmonics can be eliminated [37].

8.2.2.2 High switching frequency PWM

At high switching frequencies, the semiconductor switches perform multiple commutations
in one period of the output voltage.

- Space Vector PWM

This modulation technique provides with redundant switch states. For an m-level converter
there are \((m - 1)^3\) redundant switching states [37]. Like with a two-level converter where
the two nearest voltage vectors are chosen with a zero vector in order to minimize the
harmonic distortion in the output voltage, the three nearest triangle vertices to a reference
point are chosen in a multilevel converter. In general it is quite complicated to select the
appropriate redundant states.

- Selective Harmonic Elimination PWM

Selective Harmonic Elimination PWM is based on step wave modulation but has the ability
to eliminate particular harmonics when the conducting angles are set accordingly. It can
be used for converters with a small number of levels with good results compared to other
two methods presented here. As the number of the level increases SPWM becomes more
efficient though. Furthermore it is complex to compute the aforementioned angles. These
two factors limit the use of this modulation technique.

- Multilevel Sinusoidal PWM (or Multilevel Carrier-based PWM)

Multilevel SPWM uses a triangular wave signal as the carrier signal and one reference
signal per phase. Two common carrier-based modulation techniques are mentioned
bellow:

- Level shifted PWM

This technique is mostly used in NPC inverters and in cascaded inverters. A drawback is
the uneven power distribution among the cells which results in high harmonic distortion.
To avoid that, a rotating carrier is used to balance the power in each cell [42].

- Phase shifted PWM

This technique offers even power distribution among the cells, so it is more common than
the level shifted PWM. The idea of this modulation strategy is to shift the phase of each
carrier so as to reduce the harmonics in the output voltage. Also, it is possible to work over
the linear region of modulation [42].

- PWM with Third Harmonic Injection

As it has already been mentioned, the range for the output voltage (phase–to-neutral) of
a 3-phase, 2-level converter is:

\[
-\frac{V_{DC}}{2} \leq V_t \leq \frac{V_{DC}}{2}
\]

(8.33)
Since:

\[ V_t = \frac{V_{DC}}{2} \cdot m, -1 \leq m \leq 1 \]  \tag{8. 34}

By injecting a third harmonic in the sinusoidal reference signal at high modulation indexes \( m_{dq} \), this range can be extended. Therefore a better DC utilization is achieved compared to SVM and SPWM. Thus, with third harmonic injection either a 15% increase can be achieved at the output converter voltage with a given DC bus or a 13% reduction at the DC bus for a specific converter output voltage [27], [37].

If \( m_a, m_b, \text{and } m_c \) where \(-1 \leq m_{abc} \leq 1\), the augmented with third harmonic signals will be:

\[ m_{aug.abc} = \frac{3}{2} m_{abc} - \frac{2}{3} \frac{m_{abc}^3}{m_d^2 + m_q^2} \]  \tag{8. 35}

Where: \(-1.15 \leq m_{abc} \leq 1.15\) for a higher AC output voltage or \(-0.869 \leq m_{abc} \leq 0.869\) for DC bus reduction.
9 SIMULATIONS

The first step of the simulation testing is to create a 3-phase system, with a shunt connected STATCOM and a wind farm and then design the controller for it. At this first stage, the STATCOM is based on a 3-phase, 2 level semi-conductor bridge. The idea is that the STATCOM will be connected at the secondary of a transformer at low voltage level and to create a power module like the ABB product PCS 100 STATCOM [43].

According to [43], up to 32 PCS 100 modules can be connected in parallel in order to increase the total power rating. So the next step of the simulations is to connect two of the 2 level modules in parallel with a common DC link so as to double the power rating. The topology will be implemented at a medium voltage power system as well with higher total power rating and without a transformer.

9.1 Converter Topologies

In Figure 9.1 the basic power module is shown which is basically a 3-phase, 2 level converter and its dynamic range for MV and LV is presented in Table 9.1.

As mentioned in the introduction above, by parallelizing two of these modules, the total dynamic range of the STATCOM will be doubled. In Table 9.2, the new dynamic range requirements are shown. From Figure 9.2 it is obvious that this topology consists of 12 switches in total.

In Table 9.3 the model’s parameters are shown, including the system’s and the converter’s parameters. In Table 9.4, the voltage stress across the semi-conductors in each position is shown. In Table 2.4, the voltage stress across the semi-conductors in each position is shown. It is very important to know how many devices in series are needed per position in order to withstand the DC link voltage. In order to calculate the needed devices in series, the voltage that they can withstand is been de-rated by 60% due to cosmic radiation. Also an extra 10% is taken into account for redundancy.

In Table 9.4 the results for the high power converter are shown. At low voltage, the voltage stress per device will be equal to 1280 V. Thus, even one 1.2 kV device will be enough.

9.2 Wind Farm Model

As mentioned in section 2.1, there are many advantages in modelling a wind farm versus single wind turbines. Although representing the whole farm a single turbine might be simpler, it does not take into account many of the park’s characteristics [17]. Moreover, using a single wind turbine model will lead to the worst case scenario and it will not be the most realistic one.

The focus of this project though is not on simulating perfectly a wind farm, but more on the control part. So the wind farm will be simulated as a load and various fault cases which will be explained further in Chapter 11 will be implemented.
Table 9.1: 2-level module - dynamic range

<table>
<thead>
<tr>
<th></th>
<th>Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV (V&lt;sub&gt;ll&lt;/sub&gt;, rms = 11000 V)</td>
<td>± 2.5 MVar</td>
</tr>
<tr>
<td>LV (V&lt;sub&gt;ll&lt;/sub&gt;, rms = 400 V)</td>
<td>± 100 kVAr</td>
</tr>
</tbody>
</table>

Table 9.2: 2 2-level modules in parallel - dynamic range

<table>
<thead>
<tr>
<th></th>
<th>Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV (V&lt;sub&gt;ll&lt;/sub&gt;, rms = 11000 V)</td>
<td>± 5 MVar</td>
</tr>
<tr>
<td>LV (V&lt;sub&gt;ll&lt;/sub&gt;, rms = 400 V)</td>
<td>± 200 kVAr</td>
</tr>
</tbody>
</table>

Figure 9.1: 2 level module

Figure 9.2: 2 2 level modules in parallel
### Table 9.3: Model’s parameters

<table>
<thead>
<tr>
<th></th>
<th>System’s Parameters</th>
<th>Converter’s Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VII,rms (V)</td>
<td>f (Hz)</td>
</tr>
<tr>
<td>MV</td>
<td>11000</td>
<td>50</td>
</tr>
<tr>
<td>LV</td>
<td>400</td>
<td>50</td>
</tr>
</tbody>
</table>

### Table 9.4: Voltage stress across the semi-conductors

<table>
<thead>
<tr>
<th>Voltage stress per device (V)</th>
<th>Si IGBT Class (kV)</th>
<th>SiC IGBT/ MOSFET Class (kV)</th>
<th>De-rated Voltage Class (kV)</th>
<th>Number of needed devices in series (+ 10% redundancy)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[VDClink]</td>
<td>4.5</td>
<td>1.7</td>
<td>3.3</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td>2.8</td>
<td>1.057</td>
<td>2.053</td>
<td>4.043</td>
</tr>
</tbody>
</table>
Since the installed VSC is for reactive power compensation, it functions as a STATCOM. The controller was developed according to this requirement. It is a PQ controller and it is performed in the dq-frame [46].

10.1 Theoretical analysis

Two-dimensional frames

There are two main two-dimensional frames: the qβ-frame and the dq-frame. Both of them have the advantage of reducing the required control loops from three to two. But in the qβ-frame, the reference signals are still sinusoidal functions whereas in the dq-frame they are DC values so PI controllers can be used. Also, the time varying inductances in the abc-frame are transformed in the dq-frame to equivalent constant parameters. This is why the latter is preferred for large power system analysis [27], [44], [45].

If the space phasor \( \vec{f}(t) = f_a + jf_b \), then the qβ-to-dq transformation can be expressed as:

\[
f_d + jf_q = \vec{f}(t)e^{-j\rho(t)} = (f_a + jf_b)e^{-j\rho(t)} \tag{10.1}
\]

If \( \vec{f}(t) = \vec{f}e^{j(\omega t + \theta)} \) and \( \rho(t) \) is chosen to be equal to \( \omega t \), then \( f_d, f_q \) will be DC quantities. The actual qβ-to-dq transformation is obtained by [27]:

\[
\begin{bmatrix}
    f_d \\
    f_q \\
\end{bmatrix}
= 
R[\varepsilon(t)] 
\begin{bmatrix}
    f_a \\
    f_b \\
\end{bmatrix}
R[\varepsilon(t)] = 
\begin{bmatrix}
    \cos(\varepsilon(t)) & \sin(\varepsilon(t)) \\
    -\sin(\varepsilon(t)) & \cos(\varepsilon(t)) \\
\end{bmatrix} \tag{10.2}
\]

The abc-to-dq transformation can be performed with the Park’s matrix, \( P[\varepsilon(t)] \), as shown below [46]:

\[
\begin{bmatrix}
    f_d \\
    f_q \\
\end{bmatrix}
= 
P[\varepsilon(t)] 
\begin{bmatrix}
    f_a \\
    f_b \\
    f_c \\
\end{bmatrix}
P[\varepsilon(t)] \\
= 
\sqrt{3} 
\begin{bmatrix}
    \cos(\varepsilon(t)) & \cos(\varepsilon(t) - 120^\circ) & \cos(\varepsilon(t) - 240^\circ) \\
    \sin(\varepsilon(t)) & \sin(\varepsilon(t) - 120^\circ) & \sin(\varepsilon(t) - 240^\circ) \\
    1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\
\end{bmatrix} \tag{10.3}
\]
Power in a three-phase system

If the phase voltages and currents in a three-phase system are expressed in space vector form, the following formulas are obtained:

\[
\begin{align*}
\vec{u}_a(t) &= \vec{u}(t)e^{j0} \\
\vec{u}_b(t) &= \vec{u}(t)e^{-j120^\circ} \\
\vec{u}_c(t) &= \vec{u}(t)e^{-j240^\circ}
\end{align*}
\]

(10.4)

The three-phase active power is given by:

\[
P = \vec{u}_a(t)\vec{i}_a(t) + \vec{u}_b(t)\vec{i}_b(t) + \vec{u}_c(t)\vec{i}_c(t) = Re\left[\frac{3}{2}(\vec{u}(t)\vec{i}^*(t))\right]
\]

(10.5)

The reactive power will be:

\[
Q = Im\left[\frac{3}{2}(\vec{u}(t)\vec{i}^*(t))\right]
\]

(10.6)

The voltage and current vectors when expressed in the dq-frame will be:

\[
\vec{u}(t) = (u_d + ju_q)e^{j\rho(t)} \\
\vec{i}(t) = (i_d + ji_q)e^{j\rho(t)} \Rightarrow \vec{i}^*(t) = (i_d - ji_q)e^{-j\rho(t)}
\]

(10.7)

Thus, the system’s active and reactive power in the dq-frame are [27]:

\[
P = \frac{3}{2}[u_d i_d + u_q i_q]
\]

(10.8)

\[
Q = \frac{3}{2}[-u_d i_q + u_q i_d]
\]

(10.9)

Phase-Locked Loop (PLL)

The AC system voltage is:

\[
\vec{V}_s(t) = \vec{V}_s e^{j(\omega_0 t + \theta_0)}
\]

(10.10)

Where: \(\vec{V}_s\) is the peak line to neutral voltage

\(\omega_0\) is the AC system frequency
θ₀ is the initial angle

The AC system voltage expressed in dq coordinates will be:

\[ (V_{sd} + jV_{sq})e^{j\rho(t)} = \hat{V}_s e^{j(\omega_0 t + \theta_0)} = \hat{V}_s (\cos(\omega_0 t + \theta_0) + j \sin(\omega_0 t + \theta_0)) \]

\( (V_{sd} = \hat{V}_s \cos(\omega_0 t + \theta_0 - \rho) \)

\( (V_{sq} = \hat{V}_s \sin(\omega_0 t + \theta_0 - \rho) \) (10.11)

If \( \rho = \omega_0 t + \theta_0 \), then \( V_{sq} = 0 \). Thus, the PLL regulates \( V_{sq} \) to be equal to zero. So, when the PLL will be in steady state, the voltage is aligned with the d-axis [27]. The simplified equations for P and Q are:

\[ P = \frac{3}{2} |V_{sd}I_d| \] (10.12)

\[ Q = \frac{3}{2} [-V_{sd}I_q] \] (10.13)

**General overview of PQ controller**

As mentioned in Chapter 4, the aim of the STATCOM is to provide the needed reactive power compensation to the AC grid. In Figure 10.3 a simple representation of the modelled system is shown. The STATCOM behaves like a voltage source with a controllable output. By controlling the AC output voltage, \( V_i \), the line currents will then change because of the coupling inductances in each phase:

\[ V_L = L \frac{di}{dt} \] (10.14)

And this is how the line currents can be indirectly regulated [27], [44], [45].

**Inner control loop**

The current controller or the inner control loops do exactly that. They regulate the \( I_d \) and \( I_q \) currents by comparing them to their corresponding reference signals and by the use of PIs. So, there are two inner control loops and the gains for the PIs can be the same for both of them. The result of these loops is to obtain the two required modulation indices the \( m_d \) and \( m_q \) for the IGBT bridge in the VSC which are then being transformed into the abc-frame to create the three modulation signals, one for each phase (or for each phase leg of the IGBT bridge) that are needed in order to perform sinusoidal PWM. Then these sinusoidal signals are being compared with a triangular carrier waveform with the desired switching frequency for the IGBTs in order to generate their pulses as mentioned in chapter 8.2.1. Figure 10.2 shows how the SPWM works as well as the 6 generated pulses for the 6 IGBTs [27], [44], [45].

In Figure 10.3 point A represents where the PLL is connected to and from where the signals go into the controller. The concept for developing the existing controller is that the STATCOM should compensate for whatever happens at the PCC so the normal operation of the AC grid will not be affected. This is the worst case scenario. Normally, the grid can contribute and also there can be other compensation contribution at the PCC from other clients etc. In this project the STATCOM is controlled to cover the whole percentage of the needed reactive power at the PCC.

**Outer control loop**

In order to obtain the needed aforementioned reference signals, outer control loops are necessary. There can be two:
1.) One that will regulate the active power so it will always be zero or the DC link voltage and will generate the reference signal for the $I_d$ current. Ideally this reference should be as close to zero as possible since active power compensation is not the objective but still the STATCOM has to cover its own losses. The implemented outer control loop in this project is the one regulating the DC link voltage. It is very important that the voltage across the DC-link capacitor is controlled. Since there is not a DC power source, probable power imbalances can really affect the DC link voltage [27], [44], [45].

2.) One that will regulate the reactive power or the voltage at the PCC and will generate the reference signal for the $I_q$ current. According to the Grid Code the magnitude of the PCC voltage should be 1 p.u. [2]. Since the objective is to have full reactive power compensation from the STATCOM at the PCC, so the reactive power from the AC grid side will be 0 and thus the $I_q$ reference will be 0. For simplicity reasons, this outer loop will be omitted in this project and the $I_q$ reference will be manually set to zero. The PCC voltage is fixed since between the PCC and the grid there is no impedance, so as to focus the control on the currents from the inner loops.

The outer controller loops need to be slower than the inner controller in order to avoid inheriting possible mistakes [27], [44], [45]. If it is 5 times slower, it should be sufficient.

*Selection of DC bus voltage*

The DC bus voltage should be chosen so as the VSC can operate properly for reactive power compensation under both steady-state and dynamic conditions. As mentioned in Chapter 8.2.1:

\[
\tilde{V}_t = \frac{V_{DC}}{2} \cdot m_{abc}, -1 \leq m_{abc} \leq 1
\]  
(10. 15)

Thus, the DC bus voltage for the worst case scenario should be double the value of the AC output voltage. So, for sinusoidal PWM it will be:

\[
V_{DC} \geq 2\tilde{V}_t, -1 \leq m_{abc} \leq 1
\]  
(10. 16)

If $|m_{abc}| > 1$, then the control enters the overmodulation area which results in low-order harmonics in the AC output voltage.

From (10.16), it is understood that $\tilde{V}_t$ should be kept small. That means that the coupling inductance should be small. However, that means that the switching frequency should increase which results in higher VSC switching losses. And this is where there should be a compromise.

If third harmonic injection is implemented, the augmented modulation signals for reducing the DC bus voltage 13% will be:

\[-0.869 \leq m_{abc} \leq 0.869\]  
(10. 17)

Thus:

\[
V_{DC} \geq 2\tilde{V}_t, -0.869 \leq m_{abc} \leq 0.869
\]  
(10. 18)

According to [27], under steady-state operation, a simplified form for the amplitude of the AC output voltage is given below:

\[
\tilde{V}_t = \sqrt{V_s^2 + \left(\frac{4}{3} Lo\right)Q_s}
\]  
(10. 19)
It is obvious, that under steady-state conditions, the amplitude of the AC output voltage is mainly affected by the amount of the needed reactive power. If the transients caused by $P_s$ are included, then:

$$\tilde{V}_T = \sqrt{V_s^2 + \left(\frac{4}{3}L\omega\right)Q_s + \frac{4}{3}L\frac{dP_s}{dt}}$$

(10. 20)

Now, also the changes in $P_s$ affect the AC output voltage amplitude. The faster the changes, the higher the impact on the amplitude [27].
Figure 10.2: SPWM implementation and pulses for IGBTs
VSC overcurrent protection

It is very important that precautions are taken in order to protect the VSC from overcurrents, especially during faults. Saturation blocks are being used in order to limit the output AC currents of the converter at 1 kA [27].

10.2 Mathematical analysis and Dynamic models

Inner control loop

In order to understand how the current controller is developed, it is important to obtain the AC system’s dynamics. From Figure 10.3 it is:

\[ \vec{V}_t = \vec{V}_s + Ri + L \frac{di}{dt} \]  \hspace{1cm} (10.21)

Where:

\[ \vec{V}_s(t) = \vec{V}_s e^{j(\omega_0 t + \theta_0)} = (V_{sd} + jV_{sq}) e^{j \rho(t)} \]  \hspace{1cm} (10.22)

\[ V_{sd} = \vec{V}_s \cos(\omega_0 t + \theta_0 - \rho) \]  \hspace{1cm} (10.23)

\[ V_{sq} = \vec{V}_s \sin(\omega_0 t + \theta_0 - \rho) \]  \hspace{1cm} (10.24)

\[ \vec{i}(t) = (i_d + j i_q)e^{j \rho(t)} \]  \hspace{1cm} (10.25)

\[ \rho(t) = \omega_0 t + \theta_0 \]  \hspace{1cm} (10.26)

\[ \frac{d \rho}{dt} = \omega_0 \]  \hspace{1cm} (10.27)
Thus, it is:

$$\ddot{V}_t = \dot{V}_s + R \dot{i} + L \frac{di}{dt}$$

$$L \frac{d}{dt}(i_{dq} e^{j \omega(t)}) = -R(i_d + j i_q)e^{j \omega(t)} + (V_{td} + j V_{tq}) e^{j \omega(t)}$$

$$- (V_{sd} + j V_{sq}) e^{j \omega(t)}$$

(10.28)

The left part of (10.28) is:

$$L \frac{d}{dt}(i_{dq} e^{j \omega(t)}) = L \left[ i_{dq} \frac{d e^{j \omega(t)}}{dt} + e^{j \omega(t)} \frac{di_{dq}}{dt} \right]$$

$$= j L \omega_0 e^{j \omega(t)} (i_d + j i_q) + L e^{j \omega(t)} \frac{d}{dt} (i_d + j i_q)$$

(10.29)

So:

$$\left\{ \begin{array}{l}
L \frac{di_d}{dt} = L \omega_0 i_q - R i_d + V_{td} - V_{sd} \\
L \frac{di_q}{dt} = -L \omega_0 i_d - R i_q + V_{tq} - V_{sq}
\end{array} \right.$$

(10.30)

The controller must decouple the equations above, where:

- $i_{dq}$ are the state variables
- $V_{tdq}$ are the control inputs
- $V_{sdq}$ are the disturbance inputs.

The decoupling terms for the $i_d - loop$ and $i_q - loop$ respectively will be:

$$\mp L \omega_0 i_{qd}$$

(10.31)

So:

$$\left\{ \begin{array}{l}
L s i_d = L \omega_0 i_q - R i_d + V_{td} - V_{sd} \\
L s i_q = -L \omega_0 i_d - R i_q + V_{tq} - V_{sq}
\end{array} \right.$$

(10.32)

As mentioned in Chapter 8.2.1, the level of the AC line-to-neutral voltage output of a three-phase, 2 level converter is:

$$V_{tdq} = m_{dq} \frac{V_{dc}}{2}$$

(10.33)

Therefore, the AC system’s dynamics are:

$$m_d = \frac{i_d (L s + R) + V_{sd} - L \omega_0 i_q}{V_{dc}}$$

(10.34)

$$m_q = \frac{i_q (L s + R) + V_{sq} + L \omega_0 i_d}{V_{dc}}$$

(10.35)
Thus, the current controller with using PIs will be designed as shown below:

\[
\begin{align*}
m_d &= \frac{(i_{dref} - i_d) K_{Pd}}{V_{DC}} + V_{sd} - L\omega_0 i_q + \frac{V_{DC}}{2} \\
m_q &= \frac{(i_{qref} - i_q) K_{Pq}}{V_{DC}} + V_{sq} + L\omega_0 i_d + \frac{V_{DC}}{2}
\end{align*}
\] (10.36)

(10.37)

In order to design the PI controllers the following formulas are used:

\[
\frac{k_i}{k_p} = \frac{R}{L}, \quad \frac{1}{\tau_i}
\] (10.38)

Where \( \tau_i \) is the desired time constant of the closed-loop system [27]:

\[
G(s) = \frac{i_d(s)}{i_{dref}(s)} = \frac{1}{\tau_i + 1}, \quad 0.5 \leq \tau_i \leq 5 \text{ ms}
\] (10.39)

The control models for the inner control loops are shown in Figure 10.4 and the average model for the closed-loop system is shown in Figure 10.5.
Figure 10.4: Inner current control loops

Figure 10.5: Simplified average model of the closed-loop system for the current controller
Outer control loop

From the outer control loop for the DC link voltage that is shown in Figure 10.6 the reference for the $I_d$ current is obtained from (10.40). Figure 10.7 shows the simplified average model for the DC link voltage control.

$$ P = \frac{3}{2} [V_{dPCC} I_{dref}] \Rightarrow I_{dref} = \frac{2P}{3V_{dPCC}} \tag{10.40} $$

![Figure 10.6: Outer control loop for the DC link voltage](image)

From the outer control loop for the PCC voltage that is shown in Figure 10.8 the reference for the $I_q$ current is obtained (10.41). Figure 10.9 shows the simplified average model for the PCC voltage control.

$$ Q = \frac{3}{2} [-V_{dPCC} I_{qref}] \Rightarrow I_{qref} = -\frac{2Q}{3V_{dPCC}} \tag{10.41} $$

Where:

$$ G_p(s) = \frac{I_d(s)}{I_{dref}(s)} = \frac{1}{\tau_i + 1} \tag{10.42} $$

![Figure 10.7: Simplified average model of the closed loop system for the outer controller for the DC link voltage](image)

![Figure 10.8: Outer control loop for the amplitude of the PCC voltage](image)

![Figure 10.9: Simplified average model of the closed-loop system for the outer controller for the amplitude of the PCC voltage](image)
Lead Filter

In order to ensure a stable closed-loop system a lead filter is needed in the outer loop that regulates the DC link voltage. This filter is designed as follows [27]:

\[ F_{lead}(s) = \frac{s + \rho_1/\alpha}{\rho_1} \]  \hspace{1cm} (10.43)

\[ \delta_m = \sin^{-1}\left(\frac{\alpha - 1}{\alpha + 1}\right) \iff \alpha = \frac{-1 - \sin(\delta_m)}{-1 + \sin(\delta_m)} \]  \hspace{1cm} (10.44)

\[ \omega_c = \frac{\rho_1}{\sqrt{\alpha}} \]  \hspace{1cm} (10.45)

The filter’s pole is \( \rho_1 \), \( \alpha \) is a real constant, \( \delta_m \) is the filter’s phase in rad and \( \omega_c \) is the corresponding gain crossover frequency. The filter’s phase, \( \delta_m \), is chosen accordingly to what the phase margin of the loop should be. Here it was chosen 80°. The gain crossover frequency, \( \omega_c \), is chosen to be \( 1/5 \) of the bandwidth of the closed-loop transfer function, \( G_p(s) \). If it larger than that it will lead to excess phase lag in the loop and this should be avoided. Here it was chosen 200 rad/sec. Thus the designed filter for this project is:

\[ F_{lead}(s) = \frac{s + 17.5}{2286.01} \]  \hspace{1cm} (10.46)

10.3 Implementation for 2 2 level modules

Everything mentioned so far is for a STATCOM consisting of one three-phase, 2 level module. In order to double the power rating of the VSC system, two of these 2 level modules will be connected in parallel. When doing so, the same control module can be used for both 2 level modules. So the control module will be only repeated one time and the generated IGBT pulses will be the same for both bridges. Figure 10.10 shows the inner current control loops combined with the two outer control loops for the DC link and the PCC voltage regulation.

Figure 10.10: Combined control loops for current control and DC link and PCC voltage regulation
11 RESULTS

The controller that was developed as described in Chapter 10 was implemented in a three phase system with a shunt connected STATCOM and a connected wind farm at the PCC. The STATCOM module consists of two 2 three-phase, 2-level IGBT bridges connected in parallel as shown in Figure 9.2. Four different cases were tested and will be further explained below. The dynamic range of the converter is shown in Table 9.2. All cases will be implemented for low and medium voltage, as shown in Table 9.2.

11.1 Example with PCC voltage control

As mentioned in Chapter 10, the control loop for the PCC voltage regulation will be omitted and the controller is going to be focused on the currents. Just as an example though, in Figure 11.1 is shown the PCC voltage when there is 5% impedance between the AC grid and the PCC and the normal inductive load is connected with no faults applied. It is regulated at $11000\sqrt{3} V$.

![PCC voltage amplitude control](image)

**Figure 11.1: PCC voltage amplitude control**

11.2 Cases

- **Case 1: Dynamic Range**
  
The dynamic range of the converter is tested while the load changes from purely inductive to purely capacitive and then purely inductive again. That corresponds to the phase difference between the voltage and the current at the AC output of the converter to be $\pm 90^\circ$, as shown in Figure 11.1. So the current will lead or lag regarding to the voltage.

- **Case 2: Unbalanced load**
  
The inductive load is connected to the PCC. An extra load is being connected to one of the phases at the PCC from the load’s side. The extra load is three times bigger than the normal load.

- **Case 3: Single phase-to-ground fault**
  
The inductive load is connected to the PCC. A single-phase-to-ground fault takes place at the PCC at one of the load’s phases.
Case 4: Three phase-to-ground fault

The inductive load is connected to the PCC. A three-phase-to-ground fault takes place at the PCC at the load’s phases. By doing so, the low voltage ride through capability of the converter is being tested as shown in Figure 3.1. In Figure 11.2b the low voltage ride through profile is shown in comparison with the voltage behavior at the PCC under the three phase to ground fault.

11.3 Results – Commentary

In the following subchapters all the results are being presented. There are two figures per case and voltage rating. The first one is the reactive power flow from the AC grid and the inverter side, which shows how the inverter responds to all various load variations and whether the AC grid remains unaffected. The red line shows the needed reactive power due to the load and the possible fault. The blue line shows the reactive power flow from the inverter’s side and the black line shows the reactive power flow from the grid’s side.

The second one shows the DC link voltage so as to see the ripple during the load variations. With the red line, the reference value for the DC link voltage is shown and with
the blue line the DC link voltage. The same comments apply also for the results for Chapter 13.

11.3.1 Results – Case 1

In this section the results from testing the dynamic range of the converter are presented for low and medium voltage.

**Low Voltage**

In Figure 11.3 the reactive power flow results are shown. The load is represented with the red line, the reactive power flow from the inverter’s side with the blue line and from the grid’s side with the black line. The inverter responds really well at the load’s demands and the grid’s operation remains unaffected.

![Figure 11.3: Reactive power flow for Case 1-LV](image)

In Figure 11.4 the variations at the DC link voltage are shown for the tested case with the blue line. The reference for the DC link voltage is shown with the red line. The full inductive load results in higher DC link voltage ripple (0.3-0.4 s and 0.5-0.6 s) whereas the full capacitive load decreases the ripple (0.4-0.5 s).

![Figure 11.4: DC link voltage for Case 1-LV](image)
Medium Voltage

Like for the low voltage, the inverter manages to compensate successfully the load’s reactive power needs and the grid remains unaffected which is shown in Figure 11.5.

![Figure 11. 5: Reactive power flow for Case 1-MV](image)

In Figure 11.6 the variations of the DC link voltage are shown for medium voltage. Comparing Figures 11.4 and 11.6 there are obvious differences. Since for the two systems the system inductance differs, the DC link voltage will also behave differently.

![Figure 11. 6: DC link voltage for Case 1-MV](image)

11.3.2 Results – Case 2

In this section the results from testing the case of unbalanced load in one of the three phases are presented for low and medium voltage.
Low Voltage

In Figure 11.7 the reactive power flow is shown. With the red line, the load is represented. At 0.4 the extra load is added at one of the phases. The inverter (blue line) manages to compensate the load’s reactive power needs so as to retain safe operation at the grid side (black line).

![Figure 11.7: Reactive power flow for Case 2-LV](image)

The DC link voltage is shown in Figure 11.8, with the blue line.

![Figure 11.8: DC link voltage for Case 2-LV](image)

Medium Voltage
In Figure 11.9 the reactive power flow is shown. With the red line, the load is represented. At 0.4 the extra load is added at one of the phases. As for the low voltage, the inverter (blue line) manages to compensate the load’s reactive power needs so as to retain safe operation at the grid side (black line).

**Figure 11. 9: Reactive power flow for Case 2-MV**

The DC link voltage is shown in Figure 11.10, with the blue line.

**Figure 11. 10: DC link voltage for Case 2-MV**

11.3.3 Results - Case 3

In this section the results from testing a single-phase-to-ground fault at the load’s side are presented for low and medium voltage.
Low Voltage

In Figure 11.11 with the red line the reactive power from the load’s side is shown. At 0.41 s for 0.04 s a single phase to ground fault is simulated at the load’s side which explains the oscillations at that point. That results in an overshoot at the inverter’s side (blue line), due to high currents. Also in Figure 11.12 there is a deep voltage sag at DC link voltage during the single-phase-to-ground fault. That results in a zero AC output converter voltage and thus the converter becomes short-circuited at the AC voltage output, for the duration of the fault. After the fault the control is regained. However in a real application this is not acceptable because it means the converter is ruined.

Medium Voltage
In Figure 11.13 with the red line the reactive power from the load’s side is shown. At 0.41 s for 0.04 s a single phase to ground fault is simulated at the load’s side which explains the oscillations at that point. That results in large sag at the inverter’s side (black line), due to high currents. In Figure 11.14 there is a voltage sag at DC link voltage during the single-phase-to-ground fault, however it does not result in a zero AC output converter voltage and thus the converter remains under normal operation.

![Figure 11.13: Reactive power flow for Case 3-MV](image)

![Figure 11.14: DC link voltage for Case 3-MV](image)

11.3.4 Results - Case 4

In this section the results from testing a three-phase-to-ground fault at the load’s side are presented for low and medium voltage. Also, the converter’s response for various switching frequencies is shown as well.

Low Voltage
In Figure 11.15 when the fault is applied (0.41 s – 0.43 s) there is an overshoot both at the load’s side (red line) and at the inverter’s side (blue line). The DC link voltage ripple shown in figure 11.16 is quite large (almost 18%) which results in losing the control over the converter. Like in case 3, the control over the DC link voltage is recovered after the fault, but in a real environment, the AC voltage output should not be zero.

Medium Voltage

The same comments apply for medium voltage as well. In Figure 11.17 when the fault is applied (0.41 s – 0.43 s) there is an overshoot both at the load’s side (red line) and at the inverter’s side (blue line). The DC link voltage ripple shown in figure 11.18 is quite large.
(almost 20%) which results in losing the control over the converter, same as for the low voltage case. For this case, three different switching frequencies are being tested, (1650, 3450 and 7950 Hz), so as to understand how the switching frequency affects the DC link voltage ripple. In Figure 11.17 with red the needed reactive power is shown, with purple, black and blue the reactive power flow from the inverter’s side is shown for 1650 Hz, 3450 Hz and 7950 Hz respectively and with green, light blue and green the reactive power flow from the grid’s side is shown for 1650 Hz, 3450 Hz and 7950 Hz respectively. In Figure 11.18 with the red the reference for the DC link voltage is shown, with black the DC link voltage for 1650 Hz, with blue for 3450 Hz and with blue for 7950 Hz. For all frequencies the control over the converter is lost during the fault. After the fault, the converter recovers, but still is not acceptable.

Figure 11.17: Reactive power flow for Case 4-MV

Figure 11.18: DC link voltage for Case 4-MV
From the reactive power flow Figures 11.3, 11.5, 11.7, 11.9, in cases 1 and 2 the VSC responds very well at the load demands at the PCC at both LV and MV. In Table 11.1 all the numerical results are shown regarding the DC link voltage ripple during fault, its steady state error after the fault is cleared, its sag and the overshoot at the reactive power flow as well as its duration. Regarding the DC link voltage, at LV the steady state error is smaller than in MV when comparing Figures 11.4 with 11.6, 11.8 with 11.10, 11.12 with 11.14 and 11.16 with 11.18.

At cases 3 and 4 (Figures 11.11, 11.13, 11.15, 11.17), there are high overshoots at the reactive power flow at the converter’s side during the faults. These overshoots are a result from high currents and really low DC link voltage sags. The current is saturated at 1 kA in order to protect the semiconductors. During these faults the AC output voltage of the converter becomes zero, since the DC link voltage has a really high deep, which results in the loss of the VSC in principle. That makes obvious the need for negative sequence injection so as to handle better the overvoltages under unsymmetrical conditions. Of course case 2 is an unbalanced situation but it does not push the converter to its limits.

Another thing that is interesting to be mentioned is the fact that an effort has been made to keep the rating of the DC capacitor (9 mF for MV and 6 mF at LV) is as low as possible and that the VSC is being used at almost its maximum reactive power compensation capability. Thus, if the load becomes half of its original rating, the DC link voltage ripple will also be half. This is shown in Figure 11.19.

![Figure 11.19: DC link voltage ripple comparison at different load conditions](image-url)

So, at full inductive load when no fault is applied, the ripple is at 1.2% and at half load it is 0.6%.
Table 11.1: Numerical results

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<td>17.5%</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
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<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
</tr>
<tr>
<td></td>
<td>0.006875%</td>
<td>0.336%</td>
<td>0.25%</td>
<td>3450</td>
<td>3450</td>
<td>3450</td>
<td>3450</td>
<td>3450</td>
<td>3450</td>
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<td>3450</td>
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</tr>
<tr>
<td></td>
<td>1.17 (0.09 s)</td>
<td>3.436 (0.09 s)</td>
<td>1.7625 (0.04 s)</td>
<td>1.25%</td>
<td>1.227%</td>
<td>17.08%</td>
<td>4.727%</td>
<td>1.25%</td>
<td>1.227%</td>
<td>17.08%</td>
<td>4.727%</td>
<td>1.25%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Case</th>
<th>LV</th>
<th>MV</th>
<th>LV</th>
<th>MV</th>
<th>LV</th>
<th>MV</th>
<th>LV</th>
<th>MV</th>
<th>LV</th>
<th>MV</th>
<th>LV</th>
<th>MV</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>17.5%</td>
<td>0.25%</td>
<td>1.7625 (0.04 s)</td>
<td>12.5%</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
</tr>
<tr>
<td></td>
<td>0.25%</td>
<td>1.7625 (0.04 s)</td>
<td>12.5%</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
<td>1650</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>LV (pu)</th>
<th>MV (pu)</th>
<th>LV (pu)</th>
<th>MV (pu)</th>
<th>LV (pu)</th>
<th>MV (pu)</th>
<th>LV (pu)</th>
<th>MV (pu)</th>
<th>LV (pu)</th>
<th>MV (pu)</th>
<th>LV (pu)</th>
<th>MV (pu)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1650</td>
<td>21%</td>
<td>0.5%</td>
<td>2.534%</td>
<td>4.76%</td>
<td>4.48%</td>
<td>12.31%</td>
<td>7.27%</td>
<td>1.273%</td>
<td>1.25%</td>
<td>1.227%</td>
<td>17.08%</td>
<td>4.727%</td>
</tr>
<tr>
<td>3450</td>
<td>20%</td>
<td>0.3%</td>
<td>4.66%</td>
<td>4.48%</td>
<td>4.48%</td>
<td>12.31%</td>
<td>7.27%</td>
<td>1.273%</td>
<td>1.25%</td>
<td>1.227%</td>
<td>17.08%</td>
<td>4.727%</td>
</tr>
<tr>
<td>7950</td>
<td>19.1%</td>
<td>0.16 s</td>
<td>2.534%</td>
<td>4.76%</td>
<td>4.48%</td>
<td>12.31%</td>
<td>7.27%</td>
<td>1.273%</td>
<td>1.25%</td>
<td>1.227%</td>
<td>17.08%</td>
<td>4.727%</td>
</tr>
</tbody>
</table>
12 CONTROLLER- NEGATIVE SEQUENCE

During asymmetric faults, the grid operation can be unbalanced. That can lead to power oscillations and large overshoots at the DC link voltage that can compromise the VSC’s normal and safe operation. By injecting the necessary negative sequence current into the grid, the unbalanced grid voltages can be controlled and thus the injected power into the grid will be regulated [44], [47], [48]. By controlling not only the positive but also the negative sequence of the currents, the large ripples at the DC link voltage due to not constant active power will be avoided. According to [47], negative sequence current injection is not yet incorporated into the Grid Code but its importance is clear. However, by injecting negative sequence current, positive sequence current control will be limited [47].

12.1 Theoretical analysis

Under balanced grid operating conditions, the AC grid voltage will not have any unbalances and thus the negative sequence component will be zero. Therefore, the references for the negative sequence currents are set to zero.

\[ I_{d,ref} = I_{q,ref} = 0 \]  \hspace{1cm} (12. 1)

When controlling both positive and negative sequence, the measured quantities are decomposed into dq components for the positive rotating frame (synchronous with the grid coordinates, \( dq^+ \)) and for the negative rotating frame (opposite rotation, \( dq^- \)). The \( dq^+ \) and \( dq^- \) will interact with each other which will result in a ripple at twice the fundamental frequency, \( 2\omega \). This second order harmonic ripple will appear in the power as well, as shown below [44], [48]:

\[ p = P_0 + P_{c2} \cos(2\omega t) + P_{s2} \sin(2\omega t) \]  \hspace{1cm} (12. 2)

\[ q = Q_0 + Q_{c2} \cos(2\omega t) + Q_{s2} \sin(2\omega t) \]  \hspace{1cm} (12. 3)

\( P_0 \) and \( Q_0 \) are the average values of the instantaneous active and reactive power respectively and \( P_{c2} \cos(2\omega t), P_{s2} \sin(2\omega t) \) and \( Q_{c2} \cos(2\omega t), Q_{s2} \sin(2\omega t) \) their second order harmonics. Moving average filters or low pass filters can be used to eliminate this ripple from the measurements. But that will add delay to the PI controller.

Since now positive and negative sequence are controlled, limiting the current into the VSC, both sequences are treated equally. Thus, the maximum current, \( i_{max} \), running through the converter will be:

\[ |i_p| + |i_n| \leq |i_{max}| \]  \hspace{1cm} (12. 4)

Where: \( i_p = i_pe^{j\omega t} \) the positive sequence current and \( i_n = i_ne^{-j\omega t} \) the negative sequence current. Figure 12.1 shows the current space vector.

![Figure 12.1: Current space vector](image-url)
12.2 Implementation for 2 2 level modules

An extra control loop will be added in parallel with positive sequence one and it will be the same with it. As mentioned before, the rotation of the negative sequence frame is the opposite from the positive sequence frame. Thus now $\omega_L$ will be a negative value. Finally the positive and negative modulation signals for the three phases will be summed up. Figure 12.2 the rotating angle of the negative sequence frame compared to the positive sequence rotating angle. Figure 12.3 shows the inner current control loops for positive and negative sequence.

![Figure 12.2: Rotating angle for positive and negative sequence frames](image)

Figure 12.2: Rotating angle for positive and negative sequence frames
Figure 12.3: Inner current control loops for positive and negative sequence
13 RESULTS

The controller that was developed as described in Chapter 12 was implemented in a three-phase system with a shunt connected STATCOM and a connected wind farm at the PCC. The STATCOM module consists of two 2 three-phase, 2-level IGBT bridges connected in parallel as shown in Figure 9.2. The four different cases that were tested before will also be implemented now as well. The dynamic range of the converter is shown in Table 9.2. All cases will be implemented for low and medium voltage, as shown in Table 9.2.

13.1 Example with PCC voltage control

As mentioned in Chapter 10, the control loop for the PCC voltage regulation will be omitted and the controller is going to be focused on the currents. Just as an example though, in Figure 13.1 is shown the PCC voltage when there is 5% impedance between the AC grid and the PCC and the normal inductive load is connected with no faults applied. It is regulated at $\frac{11000}{\sqrt{3}}$ V.

![Diagram](image)

**Figure 13.1: PCC voltage amplitude regulation**

- PCC voltage amplitude regulation comparison for the two studied control schemes.

When comparing Figures 11.1 and 13.1, it becomes obvious that when controlling only the positive sequence, the voltage ripple at the PCC is higher than when controlling both positive and negative sequence. The numerical comparison is given in Table 13.1 when there is full inductive load in the system and under no load.

<table>
<thead>
<tr>
<th>PCC voltage regulation comparison</th>
<th>PCC voltage ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Positive Sequence Control</td>
</tr>
<tr>
<td>Full Inductive Load</td>
<td>4.724%</td>
</tr>
<tr>
<td>No Load</td>
<td>1.575%</td>
</tr>
</tbody>
</table>

13.2 Cases

The same cases as in Chapter 11 are applied here as well.
13.3 Results – Case 1

In this section the results from testing the dynamic range of the converter are presented for low and medium voltage.

**Low Voltage**

In Figure 13.2 the reactive power flow results are shown. The load is represented with the red line, the reactive power flow from the inverter´s side with the blue line and from the grid´s side with the black line. The inverter responds really well at the load´s demands and the grid´s operation remains unaffected.

![Figure 13.2: Reactive power flow for Case 1-LV](image)

In Figure 13.3 the variations at the DC link voltage are shown for the tested case with the blue line. The reference for the DC link voltage is shown with the red line. The full inductive load results in higher DC link voltage ripple (0.3-0.4 s and 0.5-0.6 s) whereas the full capacitive load decreases the ripple (0.4-0.5 s).

![Figure 13.3: DC link voltage for Case 1-LV](image)
**Medium Voltage**

Like for the low voltage, the inverter manages to compensate successfully the load’s reactive power needs and the grid remains unaffected which is shown in Figure 13.4.

![Q comparison](image1)

*Figure 13. 4: Reactive power flow for Case 1-MV*

In Figure 13.5 the variations of the DC link voltage are shown for medium voltage. Comparing Figures 13.3 and 13.5 there are obvious differences. Since for the two systems the system inductance differs, the DC link voltage will also behave differently.

![DC link voltage](image2)

*Figure 13. 5: DC link voltage for Case 1-MV*
13.4 Results – Case 2

In this section the results from testing the case of unbalanced load in one of the three phases are presented for low and medium voltage.

**Low Voltage**

In Figure 13.6 the reactive power flow is shown. With the red line, the load is represented. At 0.4 the extra load is added at one of the phases for 0.1 s. The inverter (blue line) manages to compensate the load’s reactive power needs so as to retain safe operation at the grid side (black line).

![Figure 13.6: Reactive power flow for Case 2-LV](image)

The DC link voltage is shown in Figure 13.7, with the blue line.

![Figure 13.7: DC link voltage for Case 2-LV](image)
Medium Voltage

In Figure 13.8 the reactive power flow is shown. With the red line, the load is represented. At 0.6 the extra load is added at one of the phases for 0.2 s. As for the low voltage, the inverter (blue line) manages to compensate the load’s reactive power needs so as to retain safe operation at the grid side (black line).

Figure 13. 8: Reactive power flow for Case 2-MV

The DC link voltage is shown in Figure 13.9, with the blue line.

Figure 13. 9: DC link voltage for Case 2-MV
13.5 Results - Case 3

In this section the results from testing a single-phase-to-ground fault at the load’s side are presented for low and medium voltage.

**Low Voltage**

In Figure 13.10 with the red line the reactive power from the load’s side is shown. At 0.41 s for 0.04 s a single phase to ground fault is simulated at the load’s side which explains the oscillations at that point. That results in an overshoot at the inverter’s side (blue line), due to high currents. Although in Figure 13.11 there is a deep voltage sag at DC link voltage during the single-phase-to-ground fault, the converter’s AC output does not become zero, so the converter remains under normal operation.

![Figure 13.10: Reactive power flow for Case 3-LV](image)

![Figure 13.11: DC link voltage for Case 3-LV](image)
Medium Voltage

In Figure 13.12 with the red line the reactive power from the load’s side is shown as for the low voltage. That results in an overshoot at the inverter’s side (blue line), due to high currents. In Figure 13.13 during the fault the overshoot at the DC link voltage is not so high (3.377%) so the converter’s AC output does not become zero and the converter remains under normal operation.

Figure 13. 12: Reactive power flow for Case 3-MV

Figure 13. 13: DC link voltage for Case 3-MV
13.6 Results - Case 4

In this section the results from testing a three-phase-to-ground fault at the load’s side are presented for low and medium voltage. Also, the converter’s response for various switching frequencies is shown as well.

**Low Voltage**

In Figure 13.14 when the fault is applied (0.41 s – 0.43 s) there is an overshoot both at the load’s side (red line) and at the inverter’s side (blue line). The DC link voltage ripple shown in figure 13.15 is close to 17% which is still big but the controller remains under normal operation.

![Figure 13. 14: Reactive power flow for Case 4-LV](image)

![Figure 13. 15: DC link voltage for Case 4-LV](image)
Medium Voltage

In Figure 13.16 when the fault is applied (0.41 s – 0.43 s) there is an overshoot both at the load’s side (red line) and at the inverter’s side (blue line). For medium voltage, the DC link ripple is reduced to almost 4% as shown in Figure 13. and the controller remains under normal operation.

**Figure 13.16: Reactive power flow for Case 4-MV**

**Figure 13.17: DC link voltage for Case 4-MV**
Various frequencies for Medium Voltage

In the following plots, 3 different switching frequencies were studied (1650, 3450 and 7950 Hz), so as to understand how the switching frequency affects the DC link voltage ripple. In Figure 13.18 with red the needed reactive power in shown, with blue, purple and green the reactive power flow from the inverter’s side is shown for 1650 Hz, 3450 Hz and 7950 Hz respectively and with black, light blue and pink the reactive power flow from the grid’s side is shown for 1650 Hz, 3450 Hz and 7950 Hz respectively. In Figure 13.19 with the red the reference for the DC link voltage is shown, with blue the DC link voltage for 1650 Hz, with pink for 3450 Hz and with green for 7950 Hz. For all tested frequencies the converter works normally.

Figure 13. 18: Reactive power flow for Case 4-MV

Figure 13. 19: DC link voltage for Case 4-MV
13.7 Discussion

From the reactive power flow in Figures 13.2, 13.4, 13.6, 13.8, in all cases the VSC responds very well at the load demands at the PCC at both LV and MV. In Figure 13.19, at case 4, it is obvious that the DC link voltage ripple does not have big differences for the various switching frequencies and it is small (<2 %) for all three switching frequencies.

At cases 3 and 4 and especially at MV (Figures 13.12, 13.16), the overshoots at the reactive power flow at the converter’s side during the faults are limited compared with the case where only positive sequence is controlled. These overshoots are a result from high currents. The current is saturated at 1 kA in order to protect the semiconductors. While injecting negative sequence, during these faults the VSC is not short-circuited since the AC output voltage of the converter now remains in the normal operational levels. That is due to the fact that the DC link voltage has a small ripple with an almost insignificant deep during the fault. In Table 13.2 all the numerical results are shown regarding the DC link voltage ripple during fault, its steady state error after the fault is cleared, its sag and the overshoot at the reactive power flow as well as its duration.

<table>
<thead>
<tr>
<th>Table 13.2: Numerical Results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Case 1</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Case 2</strong></td>
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<tr>
<td></td>
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<tr>
<td><strong>Case 3</strong></td>
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<td></td>
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<tr>
<td><strong>Case 4</strong></td>
</tr>
<tr>
<td><strong>MV</strong></td>
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</tbody>
</table>
In this chapter all the aforementioned results will be analysed.

14.1 Discussion of results

Tables 14.1, 14.2 and 14.3 are comparative tables for a better understanding of the results in Chapters 11 and 13.

Table 14.1: DC link voltage ripple in percentage for all various studied cases (%)

<table>
<thead>
<tr>
<th></th>
<th>Positive Sequence</th>
<th>Positive and Negative Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>LV</td>
<td>5.625</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>1.736</td>
</tr>
<tr>
<td>Case 2</td>
<td>LV</td>
<td>4.125</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>1.727</td>
</tr>
<tr>
<td>Case 3</td>
<td>LV</td>
<td>19.92</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>5.86</td>
</tr>
<tr>
<td>Case 4</td>
<td>LV</td>
<td>17.5</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>1650 Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>21</td>
</tr>
</tbody>
</table>

Table 14.2: DC link voltage steady-state error in percentage after fault is cleared (%)

<table>
<thead>
<tr>
<th></th>
<th>Positive Sequence</th>
<th>Positive and Negative Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>LV</td>
<td>0.075</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>0.136 ($t_{\text{clear}} &gt; 1.2 , \text{ms}$)</td>
</tr>
<tr>
<td>Case 2</td>
<td>LV</td>
<td>0.0125 ($t_{\text{clear}} &gt; 1.2 , \text{ms}$)</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>0.182</td>
</tr>
<tr>
<td>Case 3</td>
<td>LV</td>
<td>0.006875 ($t_{\text{clear}} &gt; 1.2 , \text{ms}$)</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>0.336 ($t_{\text{clear}} &gt; 1.2 , \text{ms}$)</td>
</tr>
<tr>
<td>Case 4</td>
<td>LV</td>
<td>0.25 ($t_{\text{clear}} = 1.6 , \text{ms}$)</td>
</tr>
<tr>
<td></td>
<td>MV</td>
<td>1650 Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5</td>
</tr>
</tbody>
</table>
Table 14.3: Inverter’s overshoot during reactive power compensation in p.u.

<table>
<thead>
<tr>
<th></th>
<th>Positive Sequence</th>
<th>Positive and Negative Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>0.315 (0.025 s)</td>
<td>0.155 (0.02 s)</td>
</tr>
<tr>
<td>MV</td>
<td>0.3564 (0.03 s)</td>
<td>0.2874 (0.0175 s)</td>
</tr>
<tr>
<td>Case 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>0.29 (0.02 s)</td>
<td>0.29 (0.02 s)</td>
</tr>
<tr>
<td>MV</td>
<td>0.3908 (0.02 s)</td>
<td>0.27 (0.065 s)</td>
</tr>
<tr>
<td>Case 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>1.17 (0.09 s)</td>
<td>1.135 (0.075 s)</td>
</tr>
<tr>
<td>MV</td>
<td>3.436 (0.09 s)</td>
<td>1.4 (0.04 s)</td>
</tr>
<tr>
<td>Case 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>1.7625 (0.04 s)</td>
<td>1.76 (0.04 s)</td>
</tr>
<tr>
<td>MV</td>
<td>1650 Hz 3450 Hz 7950 Hz</td>
<td>1650 Hz 3450 Hz 7950 Hz</td>
</tr>
<tr>
<td></td>
<td>4.76 (0.16 s)</td>
<td>4.66 (0.11 s) 4.48 (0.09 s)</td>
</tr>
<tr>
<td></td>
<td>4.44 (0.044 s)</td>
<td>4.3 (0.0434s) 4.24 (0.043 s)</td>
</tr>
</tbody>
</table>

Table 14.4: DC link voltage sag (%)

<table>
<thead>
<tr>
<th></th>
<th>Positive Sequence</th>
<th>Positive and Negative Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>2</td>
<td>4.625</td>
</tr>
<tr>
<td>MV</td>
<td>1.273</td>
<td>0.841</td>
</tr>
<tr>
<td>Case 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>3.625</td>
<td>3.625</td>
</tr>
<tr>
<td>MV</td>
<td>1.227</td>
<td>0.8455</td>
</tr>
<tr>
<td>Case 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>17.08</td>
<td>16.875</td>
</tr>
<tr>
<td>MV</td>
<td>4.727</td>
<td>1.636</td>
</tr>
<tr>
<td>Case 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LV</td>
<td>12.5</td>
<td>12.3125</td>
</tr>
<tr>
<td>MV</td>
<td>1650 Hz 3450 Hz 7950 Hz</td>
<td>1650 Hz 3450 Hz 7950 Hz</td>
</tr>
<tr>
<td></td>
<td>12.31</td>
<td>7.27 7.27 4.15 3.973 3.959</td>
</tr>
</tbody>
</table>

From Table 14.1 especially for cases 3 and 4 where the system is under unbalanced conditions and the converter it pushed to its limits, it is obvious that by controlling both positive and negative sequence the DC link voltage ripple is reduced. When comparing Figures 11.4, 11.6, 11.8, 11.10, 11.12, 11.14, 11.16 and 11.18 with Figures 13.3, 13.5, 13.7, 13.9, 13.11, 13.13, 13.15, 13.17 one by one it is clear that the DC link voltage sag is always significantly smaller when controlling both positive and negative sequence. This is also shown in Table 14.4. Thus, the converter manages not to be short circuited during the fault and to operate normally. However, for case 4 at MV, the ripple is higher than 10%, but the controller is under normal operation during the fault when controlling both sequences and short-circuited when controlling only the positive sequence since the DC
link voltage has a really big sag during the fault. Furthermore, for higher switching frequencies, the ripple decreases. This is expected since the switches respond faster.

From Table 14.2 regarding the steady-state error, when controlling both positive and negative sequence it is smaller than when controlling only the positive sequence. Moreover with only positive sequence the system is not always capable to reach steady-state fast enough (<0.2 ms after the fault is cleared).

Regarding the overshoot at the reactive power flow (Table 14.3), as mentioned before it is a result of high currents into the converter. These currents are being saturated for the converter’s protections at 1 kA. But still, when controlling both sequences there is saturation for less time than controlling only the positive sequence. These times are shown in parentheses in Table 14.3.

From Figure 11.17 it is understood that for higher switching frequencies, the VSC performs significantly better. Also during the severe faults, for higher switching frequency the DC link voltage sag is not as deep which affects the normal operation of the converter. From Figure 13.19 though when controlling positive and negative sequence, higher switching frequency does not affect the DC link voltage ripple so dramatically. Nevertheless, the converter is working properly even in the lowest switching frequency that was tested (1650 Hz).

Figures 14.1, 14.2, 14.3 and 14.4, 14.5, 14.6 are comparative figures for a better understanding of the results in Chapters 11 and 13 for the DC link voltage ripple and the reactive power flow respectively including both control schemes. In Figure 14.1 the comparison of the DC link voltage ripple is shown when controlling only the positive sequence and both positive and negative sequence for case 3 for MV. In Figure 14.2 and 14.3 the same thing is shown for case 4 for MV for 1650 Hz switching frequency and 7950 Hz respectively. In Figure 14.4 the comparison of the reactive power flow is shown when controlling only the positive sequence and both positive and negative sequence for case 3 for MV. In Figure 14.5 and 14.6 the same thing is shown for case 4 for MV for 1650 Hz switching frequency and 7950 Hz respectively.

![Figure 14.1: DC link voltage ripple for case 3 - MV](image-url)
Figure 14. 2: DC link voltage ripple for case 4 - MV, 1650 Hz

Figure 14. 3: DC link voltage ripple for case 4 – MV, 7950 Hz
Figure 14. 4: Reactive power flow for case 3 – MV

Figure 14. 5: Reactive power flow for case 4 – MV, 1650 Hz
14.2 Conclusions

The developed controller was able to perform under all conditions when controlling both positive and negative sequence. The need and importance of controlling both sequences is clear since the control over the VSC is never lost and the latter is always under normal operation.

When comparing the designed controller for both positive and negative sequence it is more complicated than when controlling only the positive sequence since it requires two extra loops in the inner controller as explained in Chapter 12. Nevertheless, it is worth it, since all the results are improved and the STATCOM is able to remain always under normal operation.

All the aforementioned results prove the fact that the Grid Codes should expand and incorporate negative sequence injection as well as a requirement.
In this chapter all attempts that weren’t finished due to limited time or thoughts for further research will be mentioned.

- Implement other modulation strategies besides SPWM.
- Losses calculation at full and no load. It is important to know the losses of a STATCOM at no load as well since they are being penalized.
- Harmonic and THD calculation. Since the current model does not contain any filters THD at that point is high. Thus, integration of an appropriate filter is suggested.
- Implementation of 3rd harmonic injection. Notice its effect on the DC link voltage ripple.
- Implement the controller at a chain-link STATCOM
- Work on the optimum power module. In Table 9.4, the voltage stress across the semi-conductors and the number of needed semiconductor devices in series were shown. As far as SiC devices are concerned, is not sure so far that so many devices can be connected in series. Thus, if one device per position is considered, then according to which class the device is rated for, the DC link voltage that the device can withstand can be calculated. These results are presented in Table 15.1. Now, the power rating of each VSC module it will be adjusted accordingly. That is considered to be the optimum power module, since only one device is needed per each position.

### Table 15.1: Optimum Power Module

<table>
<thead>
<tr>
<th>SiC IGBT/ MOSFET Class (kV)</th>
<th>Maximum VDClink (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.7</td>
<td>900</td>
</tr>
<tr>
<td>3.3</td>
<td>1700</td>
</tr>
<tr>
<td>6.5</td>
<td>3300</td>
</tr>
<tr>
<td>10</td>
<td>5000</td>
</tr>
<tr>
<td>13</td>
<td>6500</td>
</tr>
<tr>
<td>15</td>
<td>7500</td>
</tr>
<tr>
<td>20</td>
<td>10000</td>
</tr>
</tbody>
</table>
16 REFERENCES

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