Modeling of an IGBT and a Gate Unit

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Abstract

The purpose of this master thesis was to create a model of an IGBT in a single pulse test circuit and connect this model to a model of a Gate Unit. The IGBT model and the single pulse test circuit were both implemented in MATLAB and the Gate Unit was implemented in Simulink. The purpose of this model was to test the actions of the gate unit, so that the initial tuning could be done before going to the lab. Since no tests were performed in the lab, it was not possible to see how much of the testing that could have been done by simulations. However, the actions of the IGBT model much resembled the actions of the real component, even though some drawbacks were clear, such as the lack of tail current and tail voltage. These comparisons could be made between simulated characteristics and recordings from a previous test with the same component.

Sammanfattning

Syftet med den här masteruppsatsen var att bygga en model av en IGBT i en single pulse test circuit och koppla denna till en Gate Unit. Modellen av IGBT:n och kretsen byggdes i MATLAB och Gate Uniten byggdes i Simulink. Syftet med en dylik model var att kunna ersätta de första testen av Gate Uniten med simuleringar, för att på så vis förkorta den nödvändiga tiden i labbet. Eftersom inga laboratorietester gjordes så var det omöjligt att avgöra hur stor del avlabbstesterna som kunde ersättas med simuleringar. Men stora likheter kunde ändå konstateras mellan IGBT-modellen och verkligheten, i jämförelser med tidigare utförda tester med samma IGBT. Det bör dock påpekas att vissa skillnader var påtagliga, såsom avsaknad av tail current och tail voltage.

Keywords

IGBT model, Behavioral model, Single Pulse Test Circuit, Gate Unit model
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1 Background

The development of IGBT’s or Insulated Gate Bipolar Transistors during the past years have resulted in the use of these devices in systems for large scale power transmission, such as HVDC links or SVCs. They reach into higher and higher voltage and current ratings and are now regularly used in, for instance, ABB’s HVDC light systems. These systems contain a great number of IGBTs. In these systems, there are some kind of control device which controls the actions of the system. However, they can only decide when a certain IGBT should be turned on and a logical signal from a computer is not sufficient to turn on an IGBT.

IGBT’s need certain care during switching. Since these devices handle current in the range of kA, they could not be turned on or turned off too fast, since this would destroy the IGBT or other components in the system. But on the other hand, a too slow turn off would result in very high losses inside the device so this is not a good option either. Therefore, it is necessary to fit a gate unit or some other control or protection device to the IGBT, which conducts the turn on or turn off in a safe manner based on instructions from a higher level of control. But turn on and turn off is not all that the gate unit must do. It must also be able to detect errors in the IGBT. In case that the IGBT has been destroyed, the gate unit must send an alarm to the control of the system so that it could take necessary actions.

The demands on the gate unit are therefore very high. The IGBT is a nonlinear device, which makes it hard to characterize and control it. The gate unit will also need to be fast, since switching times are in the range of µs. Because of this, great care has to be put into the design of the gate unit. Today, a great deal of the tuning of the gate unit is done manually in a lab, which is time consuming and takes a lot of time. Therefore it would be a great advantage to be able to simulate the actions of the gate unit and the IGBT.

The level of control and functionality in the gate unit has increased over the years. To control the speed of the turn on and turn off, it is necessary to control the increase of the gate emitter voltage. In earlier gate units, current sources together with capacitors were used to give the proper \( dU_{GE}/dt \). This is not a very accurate way of controlling an IGBT. This design also often requires the use of snubber circuits to protect the IGBT. With the construction of a new gate unit, the hopes are that these could be omitted.

The new gate unit is based on an FPGA, which acts as the “brain” of the device. The control logics are all implemented in the FPGA, which receives turn on or turn off orders, voltage measurements and decides what to do. The gate unit is also provided with voltage measurements of the gate emitter and the collector emitter voltage, current sources, voltage sources and auxiliary equipment for the functionality of the gate unit, such as communication equipment and power sources. Another feature of the gate unit is it’s self learning capabilities. It adapts some of the current levels and after a number of switching cycles, these values results in a smoother operation with less adjustments of the currents.
2 Introduction

2.1 Purpose

The purpose of this master thesis was to make a model of an IGBT in a single pulse test circuit, equipped with a gate unit. This model should be used for single pulse test circuit simulations and the model should be implemented in Matlab and Simulink. It was also required that parameter extraction should be included, which meant that a regular data sheet for the IGBT should be sufficient for the parameter extraction.

A single pulse test circuit is a circuit which is used to test IGBT’s, i.e. a commonly used test bench circuit which consists of an IGBT, an inductive load in parallel with a free wheeling diode and some stray inductance. By doing test’s in a single pulse test circuit it is possible to see how the IGBT and the gate unit interact and if the gate unit is capable of controlling the IGBT in a safe way. The test circuit is also used to optimize the performance of the gate unit and the IGBT.

To be able to do realistic simulations, accurate modeling of the components are required. There is a lot of different models in the literature. The most advanced of these models adapt physical modeling, such as the Hefner model [1]. This type of models result in very accurate simulations. However, they are very complex and require a very good knowledge about a particular IGBT, a lot of different device-specific parameters needs to be known. The intention in this work was, as mentioned, to create a model which would be rather simple to use and therefore behavioral modeling was adapted. There are a great variety of behavioral models as well, but this work was based on the models presented in [2] and [3]. The design of the gate unit was done by ABB and for more details regarding this particular gate unit see [7].

The model turned out to be quite accurate. The overall behavior was good. However, the model characteristics were not able to model the tail current during turn off or the tail voltage during turn on. But from the gate unit’s point of view, these characteristics are not of great importance, since these behaviors occur at the end of the switching, at a time where the gate unit has done it’s job.

The model of the test circuit was implemented as a matlab function and the gate unit model as a simulink program. The matlab function was then accessed by a matlab block inside the simulink program. This simulink program was then provided with a user friendly interface, developed by Viktor Rudolf, however, this was not part of the thesis work. Therefore, details regarding this work is excluded from the report.

2.2 Report Structure

The first sections, 3, 4 and 5 describe the structure of the test circuit, the IGBT model and the diode model. The next two sections, 6 and 7, give the theory and the ideas regarding the switching and describe the function of the gate unit. Section 8 describes how the whole system was implemented in Simulink and Matlab and the results of these simulations are presented in section 9. Then follows the discussion, the conclusions and some thought regarding future work.
in section 10, 11 and 12.
3 Test Circuit

3.1 The Single pulse test

To test the behavior of an IGBT it is common to use a so called single pulse test. This test is conducted to study the switching performance of the device. The test circuit is shown in figure 1. A normal test procedure is conducted as follows. The IGBT is first turned on. This will lead to an increasing current $I_L$ in the inductor. When the IGBT is turned off, the current will commute to the free wheeling diode. At this point, the test could begin. Now the IGBT is turned on, which will commute the load current in the inductance from the diode to the IGBT. Then, the IGBT is turned off and the current commutes back. Since the inductor is sufficiently large, the resistive part of the load is much smaller and the switching times are comparably short, the current drop in the load current is rather small.

![Figure 1: The single pulse test circuit as it was implemented.](image)

The purpose of this test is to study the performance of the IGBT. A typical voltage and current waveform from an IGBT can be seen in figure 2. As can be seen in the figure, both voltage and current values are quite high during switching. This results in high losses and therefore it is important to minimize the switching time. However, a too fast switching time will lead to very high $di/dt$ and $du/dt$ which can be harmful for both the IGBT and other parts of the circuit. If the $di/dt$ is too high during turn on, the reverse voltage over the diode will go very high very fast. This will lead to a high reverse current in the diode for a short time. If this current is too high it might be harmful for
the diode. During turn off, the big issue is to minimize the over voltage peak, which could destroy the IGBT if it becomes too high. This is done by keeping the $du/dt$ low. These procedures will be further described later.

![Figure 2](image.png)

Figure 2: An example of a real turn off at 3 kV and 4 kA. The blue curve corresponds to a temperature of 25 °C and the blue one at 125 °C.

### 3.2 Application of Kirchhoff’s laws

The test circuit that was used is shown in figure 1. To describe this system mathematically the Kirchhoff’s voltage and current laws could be written according to equation (1) to (5). The different voltages and currents are easiest understood by considering the markings in figure 1 and 3. As can be seen in the figures, the IGBT is modeled as a current source which is surrounded by capacitors. The modeling of the IGBT itself is considered in section 4.

\[
U_{\text{power}} = u_s + u_L + u_{CE} \quad (1)
\]

\[
u_{CE} = u_{CG} + u_{GE} \quad (2)
\]

\[
i_S = i_L + i_D \quad (3)
\]

\[
i_{GE} = i_{CG} + i_G \quad (4)
\]

\[
i_S = i_{CG} + i_C + i_{CE} \quad (5)
\]

Since there are both 3 capacitors and 2 inductors in the circuit, 5 differential equations is also needed to describe the behavior of these components. These equations could be formulated according to equation (6) to (10). Note the $U_{CE1}$ in equation (9). It is related to the collector emitter voltage according to equation (11).

\[
u_S = R_S i_S + L_S \frac{di_s}{dt} \quad (6)
\]
\[ u_L = R_L i_L + L_L \frac{di_L}{dt} \]  \hspace{1cm} (7)

\[ i_{CG} = C_{CG} \frac{du_{CG}}{dt} \]  \hspace{1cm} (8)

\[ i_{CE} = C_{CE} \frac{du_{CE1}}{dt} \]  \hspace{1cm} (9)

\[ i_{GE} = C_{GE} \frac{du_{GE}}{dt} \]  \hspace{1cm} (10)

\[ u_{CE} = u_{GE1} + i_{CE} R_{CE} \]  \hspace{1cm} (11)
4 The IGBT model

4.1 Different IGBT models

Semiconductor devices are very nonlinear and their behavior is not easy to model. Therefore a great variety of models for the IGBT has been proposed. Some, like the Hefner model [1] adapt physical modeling. This approach generally gives good results. Another advantage with these models is that they are valid for a great range of operation. However, they are very complex and to be able to use them a lot of parameters for the IGBT, which can not be derived from the regular data sheets, needs to be known. Therefore it could be a good idea to use the approach of behavioral modeling. In this case the model itself has little to do with any physical processes inside the real component. However, if the IGBT is regarded as a black box, the behavior of this black box with three connections very much resembles the behavior of the real device.

A great variety of behavioral models has been presented in literature and for this work a model presented by Oh [2], also presented by Asparuhova [3] has been adopted. They use a Hammerstein like model, which consists of a static DC part and a dynamic part for the transient behavior. The DC model presented in [2] has been used here in the exact same way. However, the dynamics were modeled in a different way. The model used is shown in figure 3. The controlled current source is a function of the DC characteristics of the IGBT. This current source is surrounded by three capacitors and a resistor. The capacitor values of a real IGBT are dependant on the collector emitter voltage and to cater for this dependence, variable capacitors are used. The collector current function is presented in section 4.2 - 4.3 and the model of the variable capacitors is presented in section 4.4.

![Figure 3: A model of the IGBT with the capacitors and resistors for the dynamic behavior.](image-url)
4.2 The DC-model

A typical example of the DC voltage current characteristics of an IGBT is shown in figure 4. This very graphic describes the IGBT DC characteristics that were used during the simulations later on. More details regarding this particular DC characteristics will be given later. Here it is only included to give the reader the main structure.

There are several ways to describe the IGBT and one way is to describe it as a Darlington Circuit. In this configuration the input transistor is a MOSFET device and the output transistor is a PNP bipolar transistor [2]. This configuration can be seen in figure 5. In this configuration, the MOSFET drain source current $I_D$ is the base current of the bipolar transistor with current gain $\beta$. This means that the collector current $I_C$ of the IGBT could be described as (12). Further on, the MOSFET current could be described with the MOSFET equations for the saturated (13) and the linear (14) regions [2]. Here, the gate source voltage of the MOSFET is the same as the gate emitter voltage of the IGBT. The threshold voltage of the MOSFET is called $U_{Th}$ and all the other voltages are clearly marked in figure 5. If $U_{DS} < U_{DS,sat} = U_{GE} - U_{Th}$ the MOSFET operates in the linear region and otherwise it operates in the saturated region.

![Figure 4](image.png)

Figure 4: The DC characteristics of an IGBT, modeled according to the procedure described in the next section.
The results regarding the MOSFET and the BJT can now be combined. But first it is important to describe the relationship between the collector emitter voltage for the IGBT and the drain source voltage for the MOSFET. According to [2] this relationship could be described as $U_{CE} = U_D + U_{DS}$. By using this information the DC characteristics for the IGBT could be described as (15) and (16). Here $k = (1 + \beta)k_p$. In this case the condition for the device to operate in the saturated region is (17). Note that the voltage $U_D$ is the forward voltage drop of the emitter - base junction in the BJT.

$$I_C = I_D(1 + \beta)$$

(12)

$$I_D = k_p\left((U_{GE} - U_{Th})U_{DS} - \frac{U_{DS}^2}{2}\right)$$

(13)

$$I_D = k_p\left(U_{GE} - U_{Th}\right)^2$$

(14)

$$U_{CE} < U_{GE} - U_{Th} + U_D$$

(17)

### 4.3 Correctional Functions

Since the DC characteristics previously described is basically the characteristics of a MOSFET and not of an IGBT, measures could be taken to adjust these functions so that they more resemble those of an IGBT. For instance, in the MOSFET equations, the relationship between the gate emitter voltage and the collector emitter saturation voltage is not a linear function according to [2]. However, this could be somewhat compensated by two second order polynomial
functions, (18) and (19). These functions are then applied to the functions for the collector emitter current and to the saturation condition in such a way that the point for the saturation shifts, (20) and (21).

\[
f_1 = a_2 U_{GE}^2 + a_1 U_{GE} + a_0 \tag{18}
\]

\[
f_2 = b_2 U_{GE}^2 + b_1 U_{GE} + b_0 \tag{19}
\]

\[
I_{C,corr} = k f_2 \left[(U_{GE} - U_{Th})(f_1 U_{CE} - U_D) - \frac{(f_1 U_{CE} - U_D)^2}{2}\right] \tag{20}
\]

\[
I_{C,corr} = k f_2 \frac{(U_{GE} - U_{Th})^2}{2} \tag{21}
\]

The point of saturation is the point in the i-v characteristics where the collector emitter current becomes approximately independent of the collector emitter voltage. To find the six constants \(a_n\) and \(b_n\) three such points are chosen in the DC characteristics. For these three points, \(I_{C,sat}\), \(U_{CE,sat}\) and \(U_{GE}\) should be recorded. The correctional functions are then applied to (16) and (17) in such a way that the point of saturation and also the current value at that point is adjusted. This gives (22) and (23). From these equations it is possible to form two different equation systems with three equations and three unknown each.

\[
\frac{I_{C(sat)}}{f_2} = k(U_{GE} - U_{Th})^2 \tag{22}
\]

\[
f_1 U_{CE(sat)} = U_{GE} - U_{Th} + U_D \tag{23}
\]

4.4 Modeling of the Capacitors

An important part of the transient behavior of the IGBT is the different capacitors. According to [6] three different capacitors \(C_{ics}\), \(C_{oes}\) and \(C_{res}\) could be distinguished and measured. \(C_{ics}\) is the input capacitance, i.e. the capacitance which is seen by shorting the collector to the emitter and measure the capacitance between the gate and the collector/emitter. Therefore, the gate emitter and the collector gate capacitors sum up to the input capacitance \(C_{ics} = C_{GE} + C_{CG}\). The capacitances between the different connections could be seen in figure 3.

The second capacitance, the output capacitance is found by measuring the capacitance between collector and the gate, shorted to the emitter [6]. This capacitance will therefore be the sum of the collector emitter capacitance and the collector gate capacitance \(C_{oes} = C_{CE} + C_{CG}\). The third capacitance, \(C_{res}\), is measured between the collector and the gate with the emitter grounded. Therefore \(C_{CG} = C_{res}\). After some re-arrangements these relationships could be described as (24) - (26).

\[
C_{GE} = C_{ics} - C_{res} \tag{24}
\]
These three capacitances are all more or less depending on the collector emitter voltage $U_{CE}$. A typical example of the dependence of the voltage is shown in figure 6. As can be seen from the figure both $C_{oes}$ and $C_{res}$ are heavily dependent on the voltage while $C_{ies}$ is almost constant. Therefore, $C_{ies}$ is approximated as a constant for all voltages. It is also clear that the voltage dependency of $C_{res}$ and $C_{oes}$ is very nonlinear. For the very low voltage regions the capacitor values are in the range of hundreds of nF, but very fast the capacitor values drop to only a few nF. To model these quite strange looking curves could be quite complicated and therefore they are approximated with (27) and (28).

![Figure 6: An example of the capacitor curves from a real IGBT.](image)

$$C_{res}(U_{CE}) = C_{res,0}(1 + U_{CE})^{-k_{res}} + C_{res,high}$$

(27)

$$C_{oes}(U_{CE}) = C_{oes,0}(1 + U_{CE})^{-k_{oes}} + C_{oes,high}$$

(28)

For each of the capacitance functions, three different constants must be defined, $C_{x,0}$, $C_{x,high}$ and $k_x$. $C_{x,high}$ are taken so that it corresponds to the highest value in figure 6. $C_{x,0}$ is taken so that $C_{x,0} + C_{x,high}$ corresponds to the highest capacitor value in figure 6. The k value is then used as a tuning
parameter for the slope. It is impossible to fit this model exactly to these curves and therefore this parameter often needs some tuning. One way to start is to take a certain capacitor and voltage value somewhere in the middle of the curve in figure 6 and solve the equation for k, then plot the result and tune the constant by hand. An example of this model, which is used later in the simulations are shown in figure 7.

![Graph](image)

Figure 7: The approximation of the different IGBT capacitors as a function of the collector-emitter voltage.
5 Diode model

5.1 A simple Diode model

Since the diode is an important component in the single pulse test as well as in most circuits which includes power switches like IGBT’s and inductances, accurate modeling of this device is also critical. The diode is not as complex to understand as the IGBT. However, to get the transient analysis correct it is important to make a model which can describe some of the diodes transient characteristics. The simplest way to model a diode is to regard it as a short circuit in the forward direction and an open circuit in the blocking direction. A somewhat better model is to say that the diode is blocking in the back direction and that the forward current is a function of the forward voltage drop. During the first implementations of this circuit it was assumed that the diode could be described via the Schottky diode equation, which is given by (29) according to [4]. The Schottky equation has its name from the Schottky diode which has a I-V characteristics which is very similar to that of a normal pn-junction diode according to [4].

\[
I_D = I_S[e^{qV/kT} - 1]
\]

(29)

This approach depends on some rough approximations. For instance, the reverse recovery behavior of the diode is ignored. The reverse recovery of a diode is not infinitively fast which means that the diode will conduct a current in the opposite direction for a short period of time. This behavior is important to take into consideration in a single pulse test and therefore a better model, which could show this behavior, was implemented.

5.2 Diode model with reverse recovery

For high power purposes, diodes with a so called pin configuration is often used. These diodes are equipped with a wide drift region with low doping [4]. These devices work with a high level of injection of carriers in the drift region. When such a device is subjected to a reverse voltage, there will always be a lot of free charges left in this region, which have to be removed before the diode can turn off. A model which can describe this behavior would therefore be sufficient to describe the reverse recovery. The reverse recovery waveform would then look something like the current described in figure 8. A model with this characteristics, which is used here, is presented in [5]. In this model the charges in the drift region is modeled with a lumped charge method. According to [5] the diode can then be described according to (30) - (32). Here \(i_D\) is the diode current and \(u_D\) is the diode voltage. How the different constants are derived is explained in 5.3. The two charge variables \(q_E\) and \(q_M\) are two help variables used inside the model. For further details regarding the model, see [5].
Figure 8: The reverse recovery current shape in a diode model.

this figure needs to show, T0, T1, IRM, p and a

\[ i_D(t) = \frac{q_E - q_M}{T_M} \]  \hspace{1cm} (30)

\[ 0 = \frac{dq_M}{dt} + \frac{q_M}{\tau} \frac{q_E - q_M}{T_M} \]  \hspace{1cm} (31)

\[ q_E = I_s \tau [e^{\frac{u_D}{nVT}} - 1] \]  \hspace{1cm} (32)

5.3 Parameter extraction

A procedure for parameter extraction for this model is also presented in [5] and is recapitulated here as follows. To define the parameters \( I_s \), \( nVT \), \( \tau \) and \( T_M \) the i-v characteristics for the diode and a figure that shows a reverse recovery of the diode is needed. An example of a reverse recovery is shown in figure 8. From this graph the four constants \( T_0 \), \( T_1 \), \( a = \frac{di}{dt} \) and \( I_{RM} \) can be derived. It is also necessary to distinguish a point \( p \) in the graph. The derivative \( a \) is approximated as a line from the turn off point at \( t = 0 \) to \( t = T_1 \).

According to [5] the depletion of the charge \( q_M \) during the linear part of the reverse recovery can be described according to equation (33). Further on, at time \( T_1 \), \( q_E = 0 \) and \( u_D = 0 \). Applying this to equation (30) yields (34). After \( T_1 \) the reverse recovery becomes independent of the diode reverse voltage and the current can be described according to (35). Here \( \tau_{rr} \) is the time constant of the reverse recovery, which can be calculated by inserting the current and time values of the point \( p \). The time constant \( \tau_{rr} \) is related to \( \tau \) and \( T_M \) according to \( 1/\tau_{rr} = 1/\tau + 1/T_M \). Now, by combining (33), (34) and setting \( T_0 = T_1 - I_{RM}/a \) equation (36) is derived, which can be solved for \( \tau \). Thereafter \( T_M \) can be derived.

\[ q_M(t) = at[T_0 + \tau - t - \tau e^{-\frac{t}{\tau}}] \]  \hspace{1cm} (33)
\[ i(T_1) = -I_{RM} = -\frac{q_M(T_1)}{T_M} \quad (34) \]

\[ i(t) = -I_{RM}e^{-\frac{t-T_1}{\tau_{rr}}} \quad (35) \]

\[ I_{RM} = a(\tau - \tau_{rr})[1 - e^{-t/\tau}] \quad (36) \]

By combining equations (30) - (32) the i-v DC characteristics can be derived as (37). As can be seen here, by setting \( T_M = 0 \) the original Schottky equation is derived. This equation can be used to determine the parameters \( I_s \) and \( nV_T \) by inserting \( T_M \) and \( \tau \). For further details and more physical background see [5].

\[ i_D = \frac{I_s}{1 + \frac{T_M}{\tau}[e^{\frac{u_D}{nV_T}} - 1]} \quad (37) \]
6 IGBT Switching Strategy

6.1 Turn on

To switch the IGBT in a safe way it is important to do the turn on and turn off in a controlled manner. This means to keep the \( \frac{di}{dt} \) during turn on and the \( \frac{du}{dt} \) during turn off within certain limits and this will be the task for the Gate Unit. If the \( \frac{di}{dt} \) is too large, there is a risk to damage the diode. This is a consequence of the reverse recovery of the diode [7]. Since the diode cannot turn off infinitely fast, it will conduct current in the reverse direction, as was described in section 5.2. The strategy regarding the turn on and the turn off given here are described in [7].

During turn on, the IGBT will operate in the linear region. In this region, the collector emitter current \( I_C \) is independent of the collector emitter voltage \( U_{CE} \). An example of the transfer characteristics between the voltage and the current can be seen in figure 9. As can be seen in the figure, the dependence is non linear. However, it can be approximated fairly enough according to (38). Here \( k_1 \) is the transconductance in the lower voltage region, \( k_2 \) is in the higher voltage region and the constant \( V_{GE,L3} \) is the point where the Gate Unit switches between these regions.

\[
I_C = \begin{cases} 
  k_1 U_{GE} & \text{if } U_{GE} < V_{GE,L3} \\
  k_2 U_{GE} & \text{if } U_{GE} > V_{GE,L3} 
\end{cases} \tag{38}
\]

By taking the derivative of (38), (39) is derived. During the initial part of the turn on, the collector emitter voltage is approximately constant and therefore the gate emitter voltage can be described according to (40). By combining (39) and (40), (41) is derived. Hence, it is clear that \( \frac{dI_C}{dt} \) can be controlled by the gate current.
\begin{align*}
\frac{dI_C}{dt} &= k_x \frac{dU_{GE}}{dt} \quad (39) \\
\frac{dU_{GE}}{dt} &= \frac{I_G}{C_{GE}} \quad (40) \\
\frac{dI_C}{dt} &= \frac{k_x}{C_{GE}} I_G \quad (41)
\end{align*}

6.2 Turn off

During turn off there is a trade off between speed and protection. It is always important to try to turn off as fast as possible. The reason for this is that the IGBT will first leave the saturation and go into the linear region. This means high current and high voltage at the same time, which will cause significant losses. Losses will cause heat and this could destroy the IGBT. However, it is important not to turn off the device too fast. And the reason for this is that this will cause a high \( U_{CE} \) voltage pulse. In the circuit, as can be seen in figure 1, there are two inductances. The larger one is the load inductance. The current in the load inductance will commute to the free wheeling diode. However, the current in the stray inductance can not commute and therefore it has to be turned off. During this turn off, the voltage across the IGBT is approximately given by (42). From this equation it is evident that it is important to not turn off the device too fast, since this will cause a significant over voltage which also could be harmful.

\[ U_{CE} \approx U_{POW} + L_S \frac{dI_C}{dt} \quad (42) \]

During the initial part of the turn off, the gate emitter voltage will be lowered to a level which corresponds to the collector emitter current in the IGBT. This current / voltage level could be found in figure 9. When this level is reached, the gate voltage will remain at this level while the collector emitter capacitance is charged to the level of approximately \( U_{POW} \), the full blocking voltage. During the time when the gate emitter voltage is constant, almost the entire gate current will go to charge the collector emitter capacitance. The voltage relations in the IGBT can be described as \( U_{CE} = U_{GE} + U_{CG} \). By taking the derivative of this (43) is derived and here it is evident that the collector emitter voltage derivative is a function of the gate current.

\[ \frac{dU_{CE}}{dt} = \frac{dU_{CG}}{dt} \approx \frac{I_G}{C_{CG}} \quad (43) \]

When the collector emitter voltage reaches it’s off blocking level, the lowering of the collector emitter current can start and through this whole process, the derivative \( dU_{CE}/dt \) should never go over a certain maximum level. By following this condition, the voltage overshoot will be kept at a minimum during the whole turn off process. The explanation for this is that when turning off a current in an inductance, there is a certain amount of energy stored in the inductor. This energy has to go somewhere. It could be dumped in a snubber circuit but in this case it is burned inside the IGBT as an over voltage. It could be done fast by turning off the IGBT fast. This would generate a high voltage peak or it
could be done slowly which would significantly reduce the over voltage. Thus, by controlling the derivative it is possible to minimize the over voltage. In this way the largest part of the energy in the inductance is burned away. However, some of the energy will be stored in the collector emitter and the collector gate capacitances. This energy will oscillate between the capacitances in the IGBT and the stray inductances, as will be seen later.
7 The Gate Unit

The gate unit is a device which controls the IGBT. Each IGBT is provided with its own gate unit which monitors the actions of the IGBT. When the gate unit receives a turn on or turn off order, it will turn on or turn off the device in such a way that it is not destroyed. A too fast or too slow turn on or turn off could be harmful for the IGBT or for other parts of the circuit, like the free wheeling diode. The gate unit should also monitor the IGBT and in case of an error turn it off in a controlled manner. There are a lot of different reasons for errors in the IGBT, it could be a short circuit somewhere in the circuit, it could be that the IGBT has broken down or it could be something else. However, it is not the task of the gate unit to distinguish the reason for the error. In case of an error, the gate unit will try to turn off the device and then report where in the switching cycle the error occurred. Then it is up to a higher level of control to distinguish the type of error and to decide what to do. The core of the gate unit is an FPGA. This acts as the "brain" of the device. There are also measuring equipment, a current source to provide the gate current, some voltage sources which are used to clamp the gate in on or off state, voltage supply for the different parts and other equipment that are necessary for the correct behavior of the gate unit. However, in this work it is only the control logic of the IGBT which is of interest. Therefore, the function of these circuits is assumed to be ideal.

7.1 The Gate Unit structure

The control logic for the IGBT consists of instructions on how to act during different parts of the turn on/off cycle. These instructions form a state machine, which is divided into seven different major states, which are illustrated in figure 10. There is one on state, which controls the IGBT when it is on, a corresponding off state, two turn on states, which controls the turn on and three turn off states for the turn off. Each state is then divided into several substates. These seven states and their sub states are described in detail in section 7.3 to 7.9. In the real gate unit there are two additional states for a soft turn off procedure. However, these have been excluded in this model. In addition to the different states, there is also a master control and a current switch in the simulink model. The purpose of the master control is to act as a conductor and initialize the right state at the right time. Since the states give a gate current value $I_G$, the purpose of the current switch is to address the current value from the current state to the IGBT. A schematic view of the implementation of the simulink program is shown in figure 11. In this figure the seven states, the master control, the current switch and the Matlab block can be seen. The matlab function block is the interface to the matlab function which describes the test circuit. The major signal buses are also seen in this figure. There is the initialization bus for the states, the gate current bus to the current switch, the error bus and the next state bus which are used for the states to report back to the master control, feedback loops for $U_{CE}$ and $U_{GE}$ and also the on/off input signal to the master control.
Current controlled turn on

Initial Turn on

Off - State

Voltage Limited Stage

Initial turn off Stage

Voltage Controlled Stage

Figure 10: A schematic of the state machine in the gate unit.

$U_{CE} \& U_{GE}$ bus

Next state and error bus

Initialization bus

Master Control

On/Off

Current controlled turn on

Clamp on

Initial turn off

Voltage controlled turn off

Voltage limited turn off

Clamp off

$I_G$

Current Switch

MATLAB system

Figure 11: The basic layout of the Simulink program. This picture illustrates the layout of the gate unit and how the different major parts are interconnected.
7.2 Master Control

The purpose of the master control is to initialize the different states at the right time. The basic scheme of the master control can be seen in figure 12. The master control has 12 inputs. There are 7 feedback signals from all the different states, these go into the Next state register. When a state is complete it reports which state should take over the control of the IGBT by sending in a signal to the next state register. There is also an error register which goes to the error detection block and a turn on/off signal. These three signals, on/off, next state and error, go into the seven logic blocks which determines when a new state should be initialized. The logic conditions for these blocks are presented in table 1. As can be seen in this table, the error signal block disables the turn on if a fault occurs. The turn off could be initialized either in case of a turn off signal or due to an error, as can be seen in the table. It is important to note that an error could be initialized in other states than the turn on clamping state. The errors are detected by the current state and reported back to the master controls error detector.

There are eight output ports of the gate unit. Seven of these are state initialization ports and one sends the current state number to the master current switch. Inside the master control there are basically two registers and a set of logical conditions which decides which state should be initialized next. The next state register is necessary especially for the clamping states. These states will report which state that could take over long before the turn on or turn off signal comes. The initialization register is formed by the latches connected to the output ports. These latches are updated whenever a new logic block sends out a logical 1. However, if a logical block becomes zero the latches are not updated. This is important since it is very likely that all the logic blocks could send out a logical zero and this does not mean that all states should be disabled. This occurs for instance in the on or off states. During these states the logical condition for the state is no longer active, since the next state register has been updated. However, a new state will not be initialized until the turn on/off signal changes or an error occurs.
Figure 12: This is the layout of the master control. There are seven logic blocks that decides which state should be enabled.

<table>
<thead>
<tr>
<th>Logic</th>
<th>Next state</th>
<th>Turn on/off</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>1: Off state</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>2: Initial turn on</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3: Current controlled turn on</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4: On state</td>
<td>4</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5: Initial turn off</td>
<td>5</td>
<td>0 alt. 1</td>
<td>0 alt. 1</td>
</tr>
<tr>
<td>6: Voltage controlled state</td>
<td>6</td>
<td>0 alt. 1</td>
<td>0 alt. 1</td>
</tr>
<tr>
<td>7: Voltage limited state</td>
<td>8</td>
<td>0 alt. 1</td>
<td>0 alt. 1</td>
</tr>
</tbody>
</table>

Table 1: This table describes the required logical conditions for a certain state to be initialized. 1 means logical high and zero logical low. X is equivalent to the logical “don’t care” i.e. the signal could be either 0 or 1. As can be seen, the turn off could be initialized by a turn off signal (logical 0 in state 4) or an error.

7.3 Off Stage

The off stage is the simplest of all stages in the gate unit. It’s purpose is to supervise the IGBT while it is turned off. It consists of two loops. One initial loop and one while loop, in which the gate unit will remain until it receives a turn on order, as can be seen in the state machine graph in figure 14. Each loop
is implemented as a set of conditions which could be fulfilled in a certain way. When one of these two options are fulfilled, it will result in a locking of a latch which enables the next loop. Therefore, only the first loop is provided with a latch. As will be seen, these latches in combination with logical blocks are used extensively throughout the whole gate unit.

The purpose of the initial loop is to make sure that the gate emitter voltage drops down to a secure level in a specified maximum time. If this condition is fulfilled, the first latch is locked and the second loop is initialized. Otherwise, the first latch is locked in error mode. This will produce an error message and the gate current is set to its maximal negative value. The second loop is supervising both the collector emitter and the gate emitter voltage. If the collector emitter voltage is too high, the state will produce an error message. If the gate emitter voltage is too high or too low, the state will try to adjust the voltage so that it becomes approximately -5 V. A schematic of the implementation of this state machine can be seen in figure 13.

![Schematic diagram](https://via.placeholder.com/150)

**Figure 13:** This is a schematic drawing of the off state as it has been implemented in Simulink.
7.4 Initial Turn on

The purpose of the initial turn on is to raise the gate emitter voltage to the threshold voltage \([VGE_{L2}]\) in less time than \(2[T_{on1}]\). This procedure is controlled by the state machine in the initial turn on block. A flow chart of this state can be seen in figure 16. As can be seen in this figure, the state machine
consists of two major loops. One is activated if the process takes too long time. This loop will increase the current by $[\text{incr3}]$ every 200 nano seconds. The other loop is activated if the process goes too fast. In this case the current is decreased correspondingly. If the turn on or turn off takes longer time than $1.5[T_{\text{on1}}]$ or shorter time than $0.5[T_{\text{on1}}]$, an alarm flag will be sent to a higher level of control. The final value of the current from this state will also be saved and used as $[I_{\text{g1 on}}]$ during the next switching cycle.

A schematic of the implementation of this state in simulink can be seen in figure 15. It’s major components is a logic block, a current control block and a next state and error latch. In the logic block there is a set of comparators and AND gates which forms the different conditions for the different cases in the flow chart. Whenever a condition for a change of the current is activated, the corresponding output signal, there are six of them, will become high which will initialize a change of the gate current in the current control block. The initial condition for this block is $[I_{\text{g1 on}}]$. When a condition which leads to a green field in the flow chart is activated, this will give the next state and error block a signal to transmit an order to the master control to initialize a new state. If the time limit was exceeded, an error message will be produced and the master control will be ordered to go back to the clamp off state. Otherwise, the next state in the turn on process will be initialized.

\[
\begin{align*}
&U_{\text{GE}} \\
&\text{Voltage and time depending logic} \\
&\text{Current block} \\
&\text{Output latch} \\
&I_G \\
&\text{Next State} \\
&\text{Error}
\end{align*}
\]

Figure 15: This is a schematic drawing of the initial turn on state as it has been implemented in Simulink.
7.5 Current Controlled Turn on

The purpose of the current controlled turn on is to keep the $dI_C/dt$ below a certain level as described in section 6. The strategy to achieve this can be seen as a flowchart in figure 17. As can be seen in the figure, this state consists of five loops. The purpose of the two first loops are to control the raising of the gate voltage in a controlled way. The third loop is intended to lower the collector emitter voltage. This can only be done when the collector emitter current is fully on. At this point, the IGBT will go into saturation. The fourth loop makes sure that the IGBT really has gone into saturation and the purpose of the last loop is to make sure that the IGBT gate emitter voltage is raised the last volts to a proper on state level, usually 15 V. Here follows a description of
According to (41), it is possible to control the \( dI_C/dt \) by controlling the gate current. Therefore, the current \([L_{g2\,on}]\) is initially applied. This current is set to correspond to the initial transconductance \( k_1 \) and the desired derivative. At time \([T_{on2}]\), the collector emitter current should have reached a level which corresponds to \( I_C = k_1[VGE\_L3] \). At this point, the next conductance \( k_2 \) should be used. This implies that the gate current should be lowered and set to a new value. This event is detected by the second loop and a new current, \([L_{g21\,on}]\) is applied.

Since it is very hard to set the two different current levels precisely at the same time, loop 1 and 2 monitors that the voltage rise is neither too fast, nor too slow. Therefore, when the first level is reached, the clock is reset and the next voltage level is used. The idea is that the three different voltage levels should be reached on the same time and since they all correspond to an approximately equidistant current increase, the gate unit can monitor that the current rise is within the desired interval. If a certain voltage level is reached too fast, the current is decreased by \([L_{incr\,4}]\) and if the opposite event occurs, the current is increased with the same amount. The details regarding the timing of these increases and decreases can be found in figure 17.

But this approach does not cover all the possible events that could occur. If the collector emitter current is low, the gate emitter voltage will not reach the higher voltage levels at the desired time. The reason for this behavior is that the IGBT has to go into saturation before the gate emitter voltage can keep on increasing. In this case, the state will remain in Loop 1 and 2 until the time exceeds \(2[T_{on\,2}]\). Then the gate unit will proceed to loop 3 regardless if the voltage has reached \([VGE\_L5]\).

The purpose of the third loop is to take the IGBT into saturation. When the collector emitter current has reached its final level, i.e. when the whole load current has commutated from the diode to the IGBT, the collector emitter voltage must be lowered. This is done by discharging the collector gate capacitance \( C_{CG} \) with the gate current. Unless this capacitor has been discharged, the gate emitter capacitance cannot be increased. To lower the collector emitter capacitance with a reasonable derivative, the current \([L_{g22\,on}]\) is applied and the time is reset. If the time is exceeded the turn on is aborted, the negative current \([L_{g7\,off}]\) is applied and the gate unit initialize the off state. Otherwise, the state proceed to loop 4 and applies the current \([L_{g3\,on}]\).

Loop 4 is approximately the same procedure as in loop 3. However, the voltage level is much lower. \([VCE\_L1]\) is in the range of hundreds of volts while \([VCE\_sat\_L2]\) is in the range of volts. If the collector emitter voltage does not drop down to this level, this is an indication of a short circuit and the soft turn off will be initialized. (The soft turn off was not implemented in this model). The last part, loop 5, is used to raise the gate emitter voltage to the final level and then initialize the on state. If this level is not reached within a certain time, the turn off procedure is initialized and an error message is sent to a higher level of control.
The implementation of this state can be seen in figure 18. The logic block 1 contains the logic for loop 1 and 2, logic 2, for loop 3 etc. When each loop is completed, corresponding latch is locked so that the corresponding logic is disconnected. The latches can lock in fault mode and in no fault mode in the same way as previously described.
Start current controlled turn-on

Source current \([I_g1\text{on}]\)

Start time counting for \([T_{t_{\text{on}}}]\)

\(y = 3\)

Set alarm [flag7]

Loop 1

Increase current by \([I_{\text{incr}}]\)

\(t > 1.2[T_{t_{\text{on}}}]\)

No

\(V_{CG} > V_{GE_{L1}}\)

Yes

\(V_{CG} > V_{GE_{L2}}\)

No

\(t > 1.5[T_{t_{\text{on}}}]\)

No

\(t > 2[T_{t_{\text{on}}}]\)

Yes

Set alarm [flag7]

\(y = 5?\)

Yes

No

Loop 2

\(t > 1.2[T_{t_{\text{on}}}]\)

Yes

\(V_{CG} > V_{GE_{L1}}\)

No

\(t < 0.8[T_{t_{\text{on}}}]\)

Yes

\(t < 0.5[T_{t_{\text{on}}}]\)

No

Yes

\(y = 3, \text{ decrease current by } [I_{\text{incr}}]\)

No

Yes

If \(y = 3\), source current \([I_{g21\text{on}}]\)

\(y = y + 1\)

Loop 3

Source current \([I_{g22\text{on}}]\)

\(V_{CG} < V_{CE_{L1}}\)

Yes

\(t > 0.3[T_{t_{\text{on}}}]\)

No

Yes

Fault message: Turn-on aborted (time out)

Sink current \([I_{g7\text{on}}]\)

Enter turn-off gate clamping state

Fault message: Short Circuit condition

Loop 4

Source current \([I_{g3\text{on}}]\)

\(t > 1.2[T_{t_{\text{on}}}]\)

No

\(V_{CG} < V_{CE_{L3}}\)

Yes

\(V_{CG} < V_{CE_{L4}}\)

No

Yes

Start current controlled turn-on

Initiate Soft turn-off

Fault message: Short Circuit condition

Enter turn-off gate clamping state

Fault message: Short Circuit condition

Initiate initial turn-off

Error message: Gate drive error

Figure 17: The current controlled turn on flow chart.
7.6 On State

The on state consists of two parallel parts and a total of three loops. The purpose of the first loop is to monitor the collector emitter voltage. If this voltage would rise above $[V_{CE_{sat,L2}}]$ this is an indication that there is a short circuit in the system and to protect the IGBT from over currents the soft turn off will therefore be initialized immediately.

In the real device, there is always a small leakage current in the gate emitter capacitor $C_{GE}$ which will lower the gate emitter voltage slowly. Additionally, switching transients will have an impact on the gate emitter voltage and to make sure that the gate emitter voltage really settles on the right value, between $[V_{GE,L6}]$ and $[V_{GE,L7}]$, this loop is very effective. It could be noted that the transients are the only issue during simulation, since the capacitors are ideal, they do not have any leakage current.

The purpose of loop 2 is to watch the upper level and in case the voltage reaches above this level, $[V_{GE,L7}]$, the gate emitter current is decreased by one bit and the system waits for $[T_{on,L7}]$. After that the system is reset. One bit is the smallest step with which the gate current could be changed, i.e. $I_{max}/256$.

If the second loop failed to raise the gate emitter voltage, the third loop is activated. The third loop should make sure that the gate emitter voltage stays above $[V_{GE,L6}]$. If the voltage is between $[V_{GE,L6}]$ and $[V_{GE,L5}]$, the current is increased by one bit and the system waits for $[T_{on,L6}]$. If this was not sufficient, the procedure is repeated. In case that the voltage level is even lower, below $[V_{GE,L5}]$, a more significant increase, $I_{incr3}$, will take place and the system will wait for $[T_{on,L6}]$. If the voltage is below the last level, this could indicate a gate drive error, i.e. that there is something wrong with the current source or some other components in the gate unit. In this case the gate unit will produce an error message and the turn off cycle will be initialized.

A schematic of the simulink implementation of this state can be seen in figure 20. In this figure, the upper part is the $U_{CE}$ loop and the lower part is the

![Figure 18: A schematic of the current controlled turn on simulink model.](image-url)
$U_{GE}$ loop. Whenever loop 2 or 3 is initialized, the resettable latch is locked, so that the logic can not interfere with the actions of the loop. When the time has passed, the latch is reset and the state goes back to its initial condition.

Figure 19: The on state flow chart.

Figure 20: A schematic of the simulink model of the On state. The default settings in the on state is Initial turn off.
7.7 Initial Turn off

The turn off procedure of an IGBT is a trade off between speed, the $dU_{CG}/dt$ and limiting the collector emitter over voltage peak as described in section 6.2. But before the collector emitter voltage could be raised the gate emitter voltage has to be lowered so that the IGBT enters the linear mode, which is the purpose of the initial turn off state.

A flow chart of this state can be seen in figure 21. The two first loops in this state have the purpose to lower the gate emitter voltage to $[V_{GE,L4}]$ which should still correspond to a quite high load current. This action should be done at approximately $[T_{off1}]$. The time could diverge with 20 %, but if it goes too fast or too slow the current is decreased or increased by $[I_{incr1}]$. Until the next turn off, $[I_{g1,off}]$ will then be updated. The new current will be the last current level that the loop produced. However, if the time is exceeded by $2[T_{off1}]$, a fault message will be sent to a higher level of control since this is an indication that the gate unit does not have any control of the IGBT. This could for instance be the case if the IGBT has been destroyed. There is also a possibility to enter the voltage controlled state from loop 1 and the reason for this is that if the collector emitter voltage has increased above $[V_{CE,sat,L2}]$ when the gate emitter voltage is still high, this indicates that the load current is very high and that sinking of the gate voltage must be done in a slow and controlled manner even before reaching $[V_{GE,L4}]$. If this is not the case, the state proceeds to loop 3.

In the third loop, there are three possibilities. The first one is to go directly to the voltage controlled state. This action should be taken if the collector emitter voltage has started to rise and this indicates that the IGBT has gone into the linear mode and that it is time to start the controlled turn off. If the collector emitter voltage is below this value, the loop checks to see if the gate voltage is below $[V_{GE,L1}]$. This voltage level corresponds to a level way below the threshold voltage of the component and if this is the case, there is not much left to do, the IGBT is already turned off. The reason for this condition could be that the current in the device has changed direction and is flowing in the anti-parallel diode which should always be attached to the IGBT. (This diode was excluded in the model to reduce the complexity and computation time). If this is the case, the system could safely go into the turn off gate clamping state, since the IGBT has already turned off. However, if the voltage is low and the gate emitter voltage does not go down within the specified time $2[T_{off1}]$, the gate unit will produce a fault message and try to sink the gate emitter voltage with the maximum current that the current source could produce, $[I_{max}]$.

A schematic of the implementation of this block in simulink can be seen in figure 26. The first two loops are implemented in the Current logic 1 block. The outputs of this block goes into the current control block, which interprets these signals and passes these orders through the current switch to the current control which updates the gate current. When the first loops are completed the latch will lock in no fault mode or in fault mode. This will turn off the switch so that the first logic is disconnected and in the no fault case, initialize the second logic block. The second logic block will give order directly to the current switch.
and send orders regarding next state and/or fault directly. If the latch locks in fault case, this will produce an error message.

Figure 21: The initial turn off state flow chart.
7.8 Voltage controlled state

When the initial turn off state has lowered the gate emitter voltage to \( [V_{GE,L4}] \), the IGBT has entered or is about to enter the linear region. If the current is low, the IGBT could still be in the saturated region. The purpose of the voltage controlled state is to raise the collector emitter voltage to \( [V_{CE,L4}] \) in such a way that the \( \frac{dU_{CE}}{dt} \) is kept below a certain level. The level used in the simulations was \( 4kV/\mu s \). The way this is done is described in section 6.2. According to (43) it is possible to control \( \frac{dU_{CE}}{dt} \) by controlling the gate current and this is done in this state.

Since the gate unit does not have any current measurement devices, it can not tell explicitly when the current has been completely turned off. However, it can measure the gate emitter voltage and if this voltage is below the threshold value, the IGBT is considered to be turned off. This is not true in the real case, since there will be a tail current. However, the gate unit will not have any influence of this current. But if the gate emitter voltage is below the threshold voltage, the gate unit can’t affect the current and this state will then initialize the Clamping off state.

A flow chart of this state can be seen in figure 23. It consists of four different loops. The purpose of the first loop is to make sure that the IGBT has really left the saturated region of operation and the way this is done is to send the current \( [I_{g2,off}] \) which is set according to (43) so that it will match the required derivative. In case that this voltage level is not reached but the gate emitter voltage drops way below the threshold voltage, the IGBT is considered to be turned off and the Clamping off state is initialized. If neither of these voltage levels are reached at the time \( 2[T_{off3}] \), the gate unit will produce an error message and sink the maximum current \( [I_{max}] \).

The next two loops, 2 and 3, will continue to raise the collector emitter voltage. Loop 3 should be passed 3 times. Each time a new voltage reference level is
used. If these voltage levels are equally distributed and are reached at the same
time intervals the gate unit has made sure that the derivative is constant and
kept at the desired level. If the voltage level is reached too fast, the gate current
is reduced by $[\text{Inc}_2]$ and in case it takes too long to reach a certain level, the
current is increased by the same amount. The final value of the gate current
will then be saved and used as $[\text{g}_2\text{off}]$ during the next switching cycle. If a
certain voltage level is not reached within the time $2[\text{T}_{\text{off}}]$, an error message
is produced and the maximum current will be used to try to turn it off. During
all of the iterations in these two loops the gate emitter voltage level is checked
and in case it goes below $[\text{VGE}_L1]$ the gate unit will consider the IGBT to be
turned off and the Clamp off state will be initialized.

The last loop, number four, is doing almost the same thing as the previous
two loops. However it can not change the gate current while it is waiting. This
loop is also provided with a gate emitter voltage check which can enable the
clamp off state and in case the time exceeds $2[\text{T}_{\text{off}}]$ it will produce an error
in the same way as the previous loops. If the gate emitter voltage reaches way
below the threshold voltage, this loop will initialize the clamping off state. Other-
wise, it will enter the voltage limited state as the collector emitter voltage
reaches $[\text{VGE}_L4]$. This level is set to match the voltage of the power source,$U_{\text{POW}}$.

The simulink implementation of this state can be seen in figure 24. It is
structured in the same way as the previous states. There are three different
current logic blocks with three latches. However, these can lock in three different
ways. The uppermost case initialize the next logic block, the middle enables the
next state and the lowest is the fault case. The current switch is made so that
when a latch is locked, the switch shifts to the next current logic. The different
cases and the corresponding currents can be seen in the figure.
Sink current
Start voltage controlled stage
Start time counting

Change current sink to I_{pass}

Fault message: Turn off time out

Start time counting
Sink current I_{g2 off}

Yes

> \text{2T}_{off}\%

No

Loop 1

Yes

U_{CE} < V_{GE,1}\$

No

U_{CE} > V_{CE,1}\$


Loop 2

Increase current by I_{incr2}

Yes

Set alarm [flag 3]

No

Yes

Enter turn-off gate clamping state

x = 1

No

Yes

Change current sink to I_{pass}

Fault message: Turn off time out

x = 3 + 1

Set alarm [flag 4]

Decrease current by I_{incr2}


Loop 3

Yes

\text{0.8T}_{off}\%

No

Yes

t < \text{0.5T}_{off}\%

\text{0.5T}_{off}\% 

\text{T}_{off}\%


Loop 4

Yes

Change current to I_{g7 off}

Enter turn-off gate clamping state

Enter voltage limited state

Start time counting

Yes

No

x = 3 + 1

Figure 23: The voltage controlled state flow chart.
7.9 Voltage limited state

The purpose of the voltage limited state is to keep on monitoring $dU_{CE}/dt$ during the over voltage part of the switching. This is done in a similar manner as the last loop in the voltage controlled state. However, since this state is working in the over voltage part, the $dU_{CE}/dt$ is reduced in each loop to even further reduce the over voltage. A flow chart of this state can be seen in figure 25.

As described in section 6.2, it is important to control $dU_{CE}/dt$ and in this state this is done with three equidistant collector emitter voltage levels. When one of these levels are passed, the gate current is reduced so that an ever lower derivative will be adopted during the next loop. Since the gate unit does not have any measurement of the collector emitter voltage it can not tell whether the IGBT has turned off or not and therefore the same approach is used here as in the previous state, the gate emitter voltage is checked to see if the gate voltage is way below the gate emitter voltage. If this is the case, the gate unit will not have any control of the current. If this is the case, the gate unit will sink $I_{g7,off}$ and the enter the turn off gate clamping state. The purpose of
this last current is to take down the gate emitter voltage to the off state level, usually -5 V.

This state is also provided with a clock to see that the whole process will not take longer than \([T_{\text{max,off}}]\). If it does, this means that the gate unit is not capable of turning off the IGBT. The reason for this could be that the IGBT or the gate unit has been destroyed. If this condition is fulfilled the gate unit will try to sink the maximum current \([I_{\text{max}}]\) and also produce a fault message.

In figure 26 a schematic drawing of the implementation of this state can be seen. Follows the same pattern as the previous states, with four logic blocks, for latches and a current switch. The latches in this state also contain three inputs and outputs, they can be locked in three different configurations. The uppermost line initializes the next logic, the middle one tells the initialize the off state block that the IGBT has turned off and the lowest one is the fault case. The last logic does only have two inputs and outputs, since it will never initialize another logic. The three OR blocks in the upper part of the figure detect when a certain state is completed and update the current switch in the same way as the previous states.
Start voltage limited state

Start time counting

Sink current $I_{g3\text{off}}$

$U_{CE} > V_{CE_L}$

$U_{GE} < V_{GE_L}$

$t > T_{\text{max off}}$

Change current to $I_{g4\text{off}}$

$U_{CE} > V_{CE_L}$

$U_{GE} < V_{GE_L}$

$t > T_{\text{max off}}$

Change current to $I_{g5\text{off}}$

$U_{CE} > V_{CE_L}$

$U_{GE} < V_{GE_L}$

$t > T_{\text{max off}}$

Change current to $I_{g6\text{off}}$

$U_{CE} > V_{CE_L}$

$U_{GE} < V_{GE_L}$

$t > T_{\text{max off}}$

Change current to $I_{g7\text{off}}$

Fault Message: Turn off time out

Enter turn off gate clamping state

Change current to $I_{\text{max}}$

Figure 25: The voltage limited stage.
Figure 26: A schematic of the simulink model of the voltage limited turn off state.
8 Simulation

For the simulation of the Gate Unit and the test circuit, the well known programs Matlab and Simulink were used. The Gate Unit model was built with Simulink blocks and inside the Simulink model a Matlab block was used for the simulation of the test circuit. The model was simulated in discrete time and for each time step the differential equations were linearized and new values were found according to the Euler method. Then the algebraic equations, which were the Kirshoff’s laws for the system, were solved with the Matlab solver fsolve. This was a rather time consuming approach, since fsolve is an iterative method and this system results in quite many iterations. However, it was very suitable for the interaction with the gate unit and it turned out to give rather accurate results. In this section the linearized model of the single pulse test circuit will be presented in section 8.1 and the structure of the Simulink and Matlab program will be presented in section 8.2.

8.1 The fsolve Function

The idea for solving the system of differential algebraic equations is rather simple. For each time step, the previous values of the state variables and the algebraic variables, here referred to as the unknown variables were known. Based on the previous known variables, a new set of unknown variables were guessed by the fsolve function in Matlab. These variables were sent to a Matlab function, which described the single pulse test circuit. fsolve also provided this function with the previous states, parameter values for the components, the gate current and the time step which should be used. Based on these values the new state variables were calculated according to the linearized differential equations. Based on the state variable $U_{GE}$ and the collector emitter voltage $U_{CE}$, a new value of the collector emitter current was calculated according to the DC characteristics. All of these values were then inserted into a system of linear equations, the Kirshoff’s current and voltage laws for the system, which were the actual equations that fsolve solved. So for each time step, a number of iterations had to be used and in all these iterations, new states and a new value of the collector emitter current had to be calculated. Here follows a detailed description of the whole procedure.

In the single pulse test circuit there are a total of twelve different variables which had to be calculated for each time step. There are six unknown variables, called $x$ which are shown in (44) and there are six state variables which are shown in (45). For each iteration, the previous values of all the unknown variables and all the state variables, called $x_{n-1}$ and $s_{n-1}$, were known. Based on the previous states $s_{n-1}$ and a guessed value of $x_n$, the new state variables were calculated based on Euler’s method.

$$x = [u_L \ u_S \ i_{CG} \ i_{CE} \ i_{GE} \ i_D]$$ (44)

$$s = [u_{GE} \ u_{CG} \ u_{CE1} \ q_M \ i_S \ i_L]$$ (45)

To find the new states based on Euler’s method, all the differential equations in the system had to be linearized. The differential equations for all the capacitors and inductors, (6) – (11) were linearized according to (46) – (50). These equations were solved for the unknown, i.e. the current state $s_n$. 44
The same procedure was applied to the diode, which contributed with an unknown, \( i_D \) and a state \( q_M \). By combining (30) and (31) and linearizing, (51) was derived which was solved for \( q_{M,n} \).

\[
0 = q_{M,n} - q_{M,n-1} + \frac{q_{M,n}}{\tau} - i_D
\]  

(51)

In this way, all the states were calculated based on the current "guess" of the unknown variables in the system. At this point the collector emitter current \( i_C \) was calculated according to the DC characteristics of the IGBT, which are described in (20) and (21). For the diode, a value of \( q_E \) also had to be found and it was calculated according to (32). Here it is important to note that \( u_D = -u_L \), which at this point was a known state.

Now every variable in the system was known, calculated based on the current guess. At this point the function calculated the values \( ceq \) of the algebraic equations, which should converge to zero after a number of iterations. The six algebraic equations are given in (52). When the values of all the variables in the \( ceq \) vector were within the acceptable tolerance, fsolve stopped and the Matlab block returned the \( x_n \) and \( s_n \) values to the Simulink model and the program could proceed to the next time step.

\[
\begin{pmatrix}
ceq_1 \\
ceq_2 \\
ceq_3 \\
ceq_4 \\
ceq_5 \\
ceq_6
\end{pmatrix} = 
\begin{pmatrix}
\frac{i_{S,n} - i_{D,n} - i_{L,n}}{\Delta t} \\
\frac{i_{G,n} + i_{C,n} + i_{CE,n} - i_{G,n} - i_{G,n}}{\Delta t} \\
\frac{i_{G,n} + i_{CG,n} - i_{GE,n}}{\Delta t} \\
\frac{u_{S,n} + u_{L,n} + u_{CE,n} - U_{POW}}{\Delta t} \\
\frac{u_{CG,n} + u_{GE,n} - u_{CE,n}}{\Delta t} \\
\frac{q_{E,n} - q_{M,n}}{\Delta t} + i_{D,n}
\end{pmatrix}
\]  

(52)

8.2 Structure of the Simulink Program

The schematic of the Simulink program and the exchange of the data can be seen in figure 27. For each time step \( n \), the Gate Unit decided which gate current that should be applied, based on the current state, the gate emitter and collector emitter voltages etc. This information was then passed to the Matlab block. This block also received all the previous state values \( x_{n-1} \) and \( s_{n-1} \) from the unit delay. Then the Matlab block calculated the next state as described in the previous section. These values were then sent back to the Simulink program which could then decide what to do next.
Gate Unit in discrete time

Matlab block with fsolve

$x_n = f(x_{n-1}, s_{n-1}, s_n)$

Figure 27: The structure of the Simulink and Matlab programs.
9 Results

To test the model, simulations with different load currents and supply voltages were performed. The results of these simulations are presented here in section 9.1. To see how accurate the model of the IGBT corresponds with the real device, a comparison is made between a simulation and switching characteristics from a real component is presented in section 9.2.

The IGBT that was modeled in the simulations was ABB’s 5SNA 200045K0301. This IGBT is, in reality, provided with an anti parallel diode. However, this diode was disregarded in the simulations. The same diode, though, were used as the free wheeling diode. The parameters of this component was calculated according to what was described in section 4 and the results are presented in table 2a. The values of the component in the test circuit is presented in table 2b and the parameters of the diode is presented in table 2c.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_{Th}$</td>
<td>7 V</td>
</tr>
<tr>
<td>$U_D$</td>
<td>1 V</td>
</tr>
<tr>
<td>$k$</td>
<td>250 V</td>
</tr>
<tr>
<td>$R_{CE}$</td>
<td>1 Ω</td>
</tr>
<tr>
<td>$a_0$</td>
<td>1.73</td>
</tr>
<tr>
<td>$a_1$</td>
<td>-0.21</td>
</tr>
<tr>
<td>$a_2$</td>
<td>0.01</td>
</tr>
<tr>
<td>$b_0$</td>
<td>4.23</td>
</tr>
<tr>
<td>$b_1$</td>
<td>-0.49</td>
</tr>
<tr>
<td>$b_2$</td>
<td>0.02</td>
</tr>
<tr>
<td>$C_{res,0}$</td>
<td>160 nF</td>
</tr>
<tr>
<td>$C_{res,high}$</td>
<td>3.1 nF</td>
</tr>
<tr>
<td>$k_{res}$</td>
<td>1.56</td>
</tr>
<tr>
<td>$C_{oes,0}$</td>
<td>240 nF</td>
</tr>
<tr>
<td>$C_{oes,high}$</td>
<td>8 nF</td>
</tr>
<tr>
<td>$k_{oes}$</td>
<td>1.57</td>
</tr>
<tr>
<td>$C_{ies}$</td>
<td>220 nF</td>
</tr>
</tbody>
</table>

(a) IGBT parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_S$</td>
<td>10 mΩ</td>
</tr>
<tr>
<td>$R_L$</td>
<td>0.1 Ω</td>
</tr>
<tr>
<td>$L_S$</td>
<td>20 nH</td>
</tr>
<tr>
<td>$L_L$</td>
<td>0.3 mH</td>
</tr>
<tr>
<td>$U_{POW}$</td>
<td>1.5 - 2.5 kV</td>
</tr>
</tbody>
</table>

(b) Circuit parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau$</td>
<td>770 ns</td>
</tr>
<tr>
<td>$T_M$</td>
<td>600 ns</td>
</tr>
<tr>
<td>$nV_T$</td>
<td>0.54 V</td>
</tr>
<tr>
<td>$I_0$</td>
<td>14.7 A</td>
</tr>
</tbody>
</table>

(c) Diode parameters

Table 2: Tables with all the parameters in the test circuit, including the semiconductors.

9.1 Simulations

To see the actions of the model, some simulations were done with different values of $U_{POW}$ and $I_L$, the supply voltage and the free wheeling current. The free wheeling current could be set as an initial condition. All of the simulations are approximately 7 µs long. Initially the IGBT is in off state. At 1 µs a turn on order is given to the gate unit and at 4 µs a turn off order is given. In all the simulations, there are some initial oscillations. These oscillations arise from problems with the initial conditions. Since these are not fitted exactly, the program must settle at a stable point. But since they were damped out quickly and did not interfere with the switching, they were not considered to be so bad.
Simulations with different current and voltage values were performed and the first one of these simulations can be seen in figure 28. The turn on takes about 1.5 $\mu$s and the turn off less than 1 $\mu$s. Several of the typical behaviours of the IGBT switching characteristics can be observed, such as the initial lowering of the collector emitter voltage. This behavior is caused by the $di/dt$ in the stray inductance. Also the reverse recovery current at 2 $\mu$s and the voltage overshoot at 4.5 $\mu$s. However, the tail current during the turn off and the tail voltage during turn on are absent.

![Figure 28: Switching of 2 kA at a supply voltage of 1.5 kV.](image)

Here follows three more figures for different conditions to show that the model can handle different conditions. The basic structure is the same, although some minor variations are interesting to note. Figure 29 shows a turn on at zero current. Here the voltage overshoot is minimal, since the IGBT only has to turn off approximately 30 A.
Figure 29: Switching of zero current at a supply voltage of 2.5 kV.

Figure 30 shows switching of 3 kA, which takes the component close to its maximum ratings. During this switching the voltage overshoot is much less than during the switching at 1.5 kV. At 1.5 kV the overshoot is around 500 V and at this switching the overvoltage is between 100 and 200 V. This is explained from the behavior of the gate unit. The differences between the two curves can be clearly seen in figure 31. In the case with the lower current and voltage, the gate unit never goes into the voltage limited state, since the voltage levels are not so high. But in the case with the higher voltages and currents, the gate unit goes into this state which results in a smoother overshoot.
Figure 30: Switching of 3 kA at a supply voltage of 2.5 kV.

Figure 31: A comparison between switching of 3 kA at 2.5 kV and 2 kA at 1.5 kV.
9.2 Comparison with a real switching characteristic

To be able to compare the model of the IGBT some real switch characteristics was needed. In figure 32 recordings from a lab test of one IGBT of the same model is shown. This turn on is not done with the gate unit presented here but with an older model and therefore the actions of this particular switching was replicated, i.e. the same gate current was applied to the IGBT model. The result of this action is shown in figure 33 and the gate voltage is shown in figure 34. Sadly, no recordings of the actual gate currents was available. However, with the assistance of some specifications and my supervisor att ABB, the main characteristics of this current could be reproduced.

As can be seen in the figure, the results are not the same. However, the most important features can be distinguished in the graphs. In both the real and in the simulated case, there are a fast lowering of the collector emitter voltage due to the stray inductance. The reverse recovery of the diode has similar behavior and also the rapid decay of the collector emitter voltage could be clearly seen and has similar time constants. Notable is of course that the real curves are much smoother and that the simulated curve has rather sharp edges.

Figure 32: The upper most figure shows the collector emitter voltage and current waveforms, recorded in a lab. The lowest figure shows the gate emitter voltage. The blue curves are the results from a IGBT temperature of 25 °C and the red one corresponds to a temperature of 125 °C.
The recorded curves from the turn off is displayed in figure 35 and the simulations are shown in figure 36 and 37. There are clear differences in these figures, even if the overall behavior during the initial parts are rather similar. However, the big drawback of the model can be clearly seen at the end. When the gate emitter voltage in the real device goes down to the threshold voltage, there will still be a significant collector emitter current, which de-charges the over voltage in the capacitors in the IGBT. But since the model lacks this tail current, the energy in these capacitors will oscillate between the stray inductance and the capacitors. This rather sharp turn off at 7 volts gate emitter voltage gives the model a quite snappy behavior.

To reduce this tendancy, the gate was clamped to -5 volts through a 50 mΩ resistor. However, this behavior is very much reduced by turning of the device.
in such way so that the over voltage were further reduced, which was the case in with the gate unit.

Figure 35: Recorded waveforms from a turn off procedure in a lab. The top figure shows the collector emitter voltage and current and the lower one the gate emitter voltage. The blue curves are the results from an IGBT temperature of 25 °C and the red one corresponds to a temperature of 125 °C.

Figure 36: The collector emitter voltage and current during a turn off according to the old procedure.
Figure 37: The gate emitter voltage during a turn off according to the old procedure.
10 Discussion

It is, indeed, a tricky task to model an IGBT and a gate unit. The ambition was initially to create a better model, one which would be capable of simulating the tail currents and the tail voltages. However, during the first month of the project, there were some serious issues with the simulations and the consequence of this was that the ambitions had to be lowered.

The final model, which has been presented here, are not perfect. The major drawback is the lack of tail current which I believe is the cause of the heavy oscillations in the end of the turn off, as can be seen in the comparison between the simulations and the real curves. However, these oscillations are significantly damped if the voltage is lowered and if the gate unit is used to smooth down the over voltage, as was the case when the gate unit was used. In these simulations, the oscillations are at a reasonable level.

But it is not only the oscillations that could be troublesome as a consequence of the lack of tail current and tail voltage. A rather significant tail current, at a time when the collector emitter voltage is high or a tail voltage at high current will result in losses. But since there are no tail currents or tail losses in this model, it will underestimate the losses in the IGBT. However, from a control point of view the tail phenomenas are less important, since the gate unit does not have any significant impact on them.

An important feature of this model is of course the modeling of the diode. This model is based on a lumped charged approach and is therefore closer to a real physical model than the IGBT. Since the impact of the reverse recovery on the switching of an IGBT is significant, this is a very important feature to include. The diode is put under severe stress during the reverse recovery, something that has to be taken into consideration. This would not have been possible with an ideal diode.

An important feature of the IGBT is the current gain during turn on and turn off. This is particularly important, since this is the characteristic which is used by the gate unit to control the current increase during turn on. To improve this feature, the correctional functions were introduced. These does not only adjust at which voltage saturation occurs, but also at which current level and therefore they were useful to adjust this feature. By setting these functions properly, the relationship between the gate voltage and the collector emitter current was improved.

Regarding the simulations as such, they could probably be made in a smarter way. But a simulation of about 10 µs takes about 5 minutes and since this time interval is sufficient to simulate a full cycle, this was considered to be acceptable. It should be noted that not much attention were paid to the initial conditions. These were set approximately. This resulted in some oscillations in the beginning, but they were damped out rather quickly. However, they some times triggered an over voltage fault in the gate unit if the system was set to start in the on state, with 15 volts gate emitter voltage.
11 Conclusions

Even though this model is not perfect, it can simulate the interactions of the gate unit and the IGBT in a single pulse circuit. The overall behavior of this model very much resembles the behavior of the real case. It is clear that the results from these simulations could not replace the use of actual testing. However, the results from this model could be used from start and then tuned in by the test, which was the goal for this work.

12 Future work

Especially the IGBT model could be improved. It is not likely that simulations ever could replace lab testing but it is much likely that an even better model would render even better guesses regarding the parameters in the gate unit. As a base for this work, the gate unit could be used. This part of the work could be fitted to any other simulink or matlab based single pulse test circuit.
References


[7] F. Hosini *Functional requirement specification for HV-IGBT Gate Drive Unit*, ABB internal document, No: 1JNA000094, Department; PSGS/GXT