Design of a Voltage Controlled Oscillator for Galileo/GPS Receiver

Examensarbete utfört i Elektroniksystem vid Tekniska högskolan vid Linköpings universitet
av

Deepak Murugan

LiTH-ISY-EX--11/4533--SE

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Abstract

The main aim of this thesis is to implement a voltage-controlled oscillator for a Galileo/GPS receiver with a center frequency of 1.5 GHz in 150 nm CMOS process. As the designed VCO has to be integrated in a phase locked loop, VCO gain is selected high enough for the PLL to lock even with process variations. A new state of art architecture called double harmonic tuned VCO is selected and designed for this GPS application. It uses a complex combination of inductors and capacitors to reduce phase-noise of the VCO by suppressing second harmonic oscillations in the tail node of VCO.

The designed VCO shows significant improvement in phase-noise performance compared to a normal LC tank VCO by reducing phase-noise around 4 dBc/Hz. The VCO has a phase-noise of -128 dBc/Hz at 1 MHz offset from center frequency with a power consumption of 5 mW and a tuning range of about 257 MHz for a 1 V tuning voltage range.
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# Table of Contents

Abstract........................................................................................................................................ iii

Acknowledgments......................................................................................................................... v

List of Acronyms........................................................................................................................... xiii

1 Introduction................................................................................................................................ 1
  1.1. Objective............................................................................................................................... 1
  1.2. Background.......................................................................................................................... 1
  1.3. Literature study.................................................................................................................... 3
  1.4. Voltage controlled oscillator specification........................................................................... 4
  1.5. Thesis organization.............................................................................................................. 4

2 Oscillator theory......................................................................................................................... 5
  2.1. Barkhausen criteria............................................................................................................... 5
  2.2. Oscillator classifications....................................................................................................... 6
    2.2.1. Ring oscillator.................................................................................................................. 6
    2.2.2. LC oscillator.................................................................................................................... 8
  2.3. Noise sources in oscillator................................................................................................... 9
    2.3.1. Flicker (1/f) noise.............................................................................................................. 9
    2.3.2. Thermal noise.................................................................................................................. 9
  2.4. Noise theory....................................................................................................................... 10
    2.4.1. Leeson’s proportionality.................................................................................................. 10
    2.4.2. Rael’s mixer based approach......................................................................................... 10
  2.5. Oscillator parameters.......................................................................................................... 12
    2.5.1. Center frequency............................................................................................................ 12
    2.5.2. Tuning frequency range............................................................................................... 12
    2.5.3. Tuning voltage ............................................................................................................... 13
    2.5.4. Gain of VCO.................................................................................................................. 13
    2.5.5. Phase noise................................................................................................................... 13
    2.5.6. Power dissipation........................................................................................................... 13
    2.5.7. Figure of merit (FOM).................................................................................................. 13
    2.5.8. Figure of merit with tuning range (FOMT).................................................................... 14
A.1 Verilog A model for PFD and charge pump ................................................................. i
A.2 Verilog A model for divider......................................................................................... ii
A.3 Verilog A model for VCO.......................................................................................... iii
A.4 Mathematica code to determine DHT tank's L and C................................................. iii

Appendix B ........................................................................................................................................ v

B.1 Transient response of current source with filter...................................................... v
B.2 Magnitude and phase response of buffer.................................................................. vi
B.3 Process corner for lowest tuning voltage................................................................... vii
B.4 Process corner for highest tuning voltage................................................................. viii
B.5 AC plot for quality factor of varactor....................................................................... ix
B.6 VCO output waveform with floating gate current source ....................................... ix
List of Figures

Figure 1.1: Typical GPS/Galileo receiver............................................................ 1
Figure 1.2: Frequency spectrum of ideal and real oscillator............................... 2
Figure 1.3: Effect of oscillator phase noise in receiver....................................... 2
Figure 2.1: Unity gain feedback system.......................................................... 5
Figure 2.2: Common source amplifier............................................................ 7
Figure 2.3: N-stage ring oscillator.................................................................... 7
Figure 2.4: Model of negative resistance oscillator.......................................... 9
Figure 2.5: Differential LC oscillator with tail bias......................................... 11
Figure 2.6: Phase locked loop......................................................................... 14
Figure 3.1: Basic VCO.................................................................................. 16
Figure 3.2: Ideal LC tank................................................................................ 16
Figure 3.3: Magnitude plot of inductive and capacitive reactances as a function of frequency...... 17
Figure 3.4: S-parameters setup for LC tank with 50 Ω termination.................... 18
Figure 3.5: S11 magnitude plot of LC tank ..................................................... 18
Figure 3.6: Magnitude of S11 for third HT tank............................................ 20
Figure 3.7: Third harmonic tuned tank......................................................... 20
Figure 3.8: Second harmonic tuned tank....................................................... 21
Figure 3.9: Magnitude of S11 of second harmonic tuned tank......................... 21
Figure 3.10: Double harmonic tuned tank...................................................... 22
Figure 3.11: Magnitude of S11 of second harmonic tuned tank around second harmonics...... 22
Figure 3.12: Magnitude of S11 of double harmonic tuned tank around second harmonics...... 23
Figure 3.13: S-parameters’ test setup............................................................. 23
Figure 3.14: Three different negative resistance topologies with top (PMOS) current source...... 26
Figure 3.15: Impedance seen from tank towards NMOS................................ 27
Figure 3.16: Basic current mirror................................................................... 29
Figure 3.17: Tail voltage vs tail current of basic current mirror......................... 31
Figure 3.18: High impedance current mirror................................................... 32
Figure 3.19: Ivanov's current mirror............................................................... 33
Figure 3.20: Ivanov current mirror vs basic current mirror............................. 34
Figure 3.21: Bias noise filtering technique....................................................... 35
Figure 3.22: Bias noise filtering with speed up switch..................................... 36
Figure 3.23: Output buffer with single output stage......................................... 37
Figure 4.1: Test setup for oscillator with ideal current source........................... 40
Figure 4.2: Tail node voltage of oscillator with LC tank and DHT tank............ 41
Figure 4.3: Tail node voltage of DHT oscillator with basic and Ivanov current mirror...... 42
Figure 4.4: Oscillator tuning voltage against frequency and phase noise............ 44
Figure 4.5: Corner simulation for VCO.......................................................... 45
Figure 4.6: VCO frequency for different supply voltages ................................................................. 46
Figure 4.7: VCO frequency for different reference current source ................................................. 47
Figure 4.8: Change of VCO frequency and phase noise over temperature ..................................... 48
Figure 4.9: Phase noise of VCO with DHT and SHT tank for the tuning range ............................. 49
Figure B.1: Noise filtering with and without start-up switch ......................................................... v
Figure B.2: Magnitude and phase plot of Buffer ........................................................................ vi
Figure B.3: Corner simulation with Vtune of 0.4 V ...................................................................... vii
Figure B.4: Corner simulation with Vtune of 1.4 V .................................................................... viii
Figure B.5: Quality factor of a mos varactor ............................................................................. ix
Figure B.6: DHT VCO output waveform with floating gate connection .................................... ix
List of Tables

Table 1.1: State of art comparison............................................................................................................. 3
Table 1.2: VCO specification..................................................................................................................... 4
Table 3.1: Design specification for current mirror.................................................................................... 30
Table 4.1: Comparison of LC and DHT tank with ideal current source.................................................. 41
Table 4.2: Comparison of LC and DHT tank with basic current mirror.................................................... 42
Table 4.3: Comparison of LC and DHT tank with Ivanov mirror............................................................... 43
Table 4.4: Comparison of LC and DHT tank with noise filtering technique........................................... 43
Table 4.5: Comparison of LC and DHT tank with varactors.................................................................... 43
Table 4.6: State of art comparison............................................................................................................. 50
Table 4.7: Description of different architectures....................................................................................... 51
# List of Acronyms

<table>
<thead>
<tr>
<th>What</th>
<th>Meaning</th>
<th>Where</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
<td>Chapters 1, 2, 3, 4 and 5</td>
</tr>
<tr>
<td>GPS</td>
<td>Global Positioning System</td>
<td>Chapters 1, 3 and 5</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
<td>Chapters 1, 2 and 3</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
<td>Chapters 1, 2, 3, and 4</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate frequency</td>
<td>Chapters 1, and 3</td>
</tr>
<tr>
<td>kVCO</td>
<td>Oscillator gain</td>
<td>Chapter 1</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
<td>Chapters 2, 3, and 4</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
<td>Chapters 3, and 4</td>
</tr>
<tr>
<td>DHT</td>
<td>Double Harmonic Tuned</td>
<td>Chapters 1, 3, 4 and 5</td>
</tr>
<tr>
<td>SHT</td>
<td>Second Harmonic Tuned</td>
<td>Chapters 3, 4 and 5</td>
</tr>
<tr>
<td>CS</td>
<td>Common Source</td>
<td>Chapter 2</td>
</tr>
<tr>
<td>LC</td>
<td>Inductor (L), Capacitor (C)</td>
<td>Chapters 1, 2, 3, 4 and 5</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
<td>Chapter 2</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
<td>Chapters 1, 2, 4 and 5</td>
</tr>
<tr>
<td>FOM$_T$</td>
<td>Figure of Merit with tuning range</td>
<td>Chapter 2</td>
</tr>
<tr>
<td>Q</td>
<td>Quality factor</td>
<td>Chapter 3</td>
</tr>
<tr>
<td>PSS</td>
<td>Periodic Steady State</td>
<td>Chapter 4</td>
</tr>
</tbody>
</table>
1 Introduction

1.1. Objective
The objective of this project is to study and design a voltage controlled oscillator (VCO) for a GPS/Galileo receiver with low phase noise and optimal power consumption. The designed VCO should be tested for different corners with process variations and also be checked for its tuning range to get locked in the phase locked loop (PLL).

1.2. Background
Any GPS system works on direct sequence spread spectrum transmission. The receiver receives GPS signal and correlates with locally generated replica signal with different delay until a maximum correlation between the two signal is achieved. By using the delay received from satellites, position of the receiver on earth can be found.

![Figure 1.1: Typical GPS/Galileo receiver](image.png)
Introduction

Shown in Figure 1.1 is the block diagram of typical GPS/Galileo receiver, where local oscillator along with mixer converts radio frequency (RF) to intermediate frequency (IF) signal. Local oscillator is a key component in the design of GPS receiver, since it is the performance limiting component due to its random change in frequency and phase. This change is often denoted as phase noise. Shown in Figure 1.2 is the frequency spectrum of ideal and real local oscillator whose center frequency is denoted by $f_0$. An ideal oscillator looks like a single tone in the frequency domain, whereas real oscillator skirts out for wider

![Figure 1.2: Frequency spectrum of ideal and real oscillator](image)

![Figure 1.3: Effect of oscillator phase noise in receiver](image)
frequency and this phenomenon of skirting out is measured in terms of phase noise with offset from the center frequency. This phase noise reduces the carrier tracking bandwidth and thus reducing the carrier to noise ratio [1].

In general, down-conversion of RF to IF in receivers is done by local oscillator and mixer. During this conversion, if there is a strong interferer present adjacent to the desired signal as shown in Figure 1.3, and also if the local oscillator spectrum is wide spread, the mixer down converts both desired and interfering signals. Thus the strong interferer might overlap the down converted desired signal as shown in Figure 1.3, in-turn degrading the signal to noise ratio. To avoid interference in the received signal emphasis should be given on phase-noise of the VCO design.

1.3. Literature study

In recent years several works are being carried out to improve the performance of VCO. Each work focuses on specific performance metrics of VCO, like low phase noise, larger tuning range, low power and less area. Also, figure of merit (FOM) comparison is calculated finally to have a standard comparison on different VCO. Few of the state of work architectures are taken and tabulated in Table 1.1.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Process (nm)</th>
<th>Vdd (V)</th>
<th>Power consumption (mW)</th>
<th>Center frequency (GHz)</th>
<th>Phase-noise (dBc/Hz) @ 1 MHz offset</th>
<th>FOM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>130</td>
<td>1.2</td>
<td>0.35</td>
<td>3.2</td>
<td>-117</td>
<td>-191.6</td>
</tr>
<tr>
<td>[3]</td>
<td>350</td>
<td>2.4</td>
<td>6.72</td>
<td>2</td>
<td>-126</td>
<td>-186*</td>
</tr>
<tr>
<td>[4]</td>
<td>180</td>
<td>1.5</td>
<td>1.7</td>
<td>3.5</td>
<td>-122</td>
<td>-195.7</td>
</tr>
<tr>
<td>[5]</td>
<td>180</td>
<td>1</td>
<td>4.4</td>
<td>3.2</td>
<td>-133</td>
<td>-196.6</td>
</tr>
<tr>
<td>[6]</td>
<td>180</td>
<td>1.8</td>
<td>5.4</td>
<td>2.4</td>
<td>-137</td>
<td>-197.5</td>
</tr>
<tr>
<td>[7]</td>
<td>130</td>
<td>1</td>
<td>1.4</td>
<td>5.2</td>
<td>-131**</td>
<td>-194.5</td>
</tr>
<tr>
<td>[8]</td>
<td>180</td>
<td>1</td>
<td>4.6</td>
<td>2.5</td>
<td>-134</td>
<td>-195</td>
</tr>
</tbody>
</table>

* Phase noise @ 500 kHz offset
** Quadrature VCO
1.4. **Voltage controlled oscillator specification**

The following section presents the specification of VCO for a GPS/Galileo receiver. It mainly focuses on low phase noise and oscillator gain with optimal power consumption. The specification of phase-noise is taken from [1]. The VCO is to be designed in 150 nm L-foundry technology and also be tested for different process corners to check if its gain is high enough for the PLL to get locked in all corners.

**Table 1.2: VCO specification**

<table>
<thead>
<tr>
<th>Performance parameter</th>
<th>Value</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center frequency</td>
<td>1.5</td>
<td>GHz</td>
<td>( f_0 )</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8</td>
<td>V</td>
<td>( V_{dd} )</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>11 (max)</td>
<td>mW</td>
<td>( P )</td>
</tr>
<tr>
<td>Oscillator gain</td>
<td>-</td>
<td>MHz/V</td>
<td>( k_{VCO} ), high enough for PLL to lock</td>
</tr>
<tr>
<td>Tune voltage</td>
<td>0.4 – 1.4</td>
<td>V</td>
<td>( V_{tune} )</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset</td>
<td>&lt; -124</td>
<td>dBc/Hz</td>
<td></td>
</tr>
</tbody>
</table>

1.5. **Thesis organization**

The thesis is organized in various chapters. Chapter 2 analyzes the theory of oscillator and noise theory. Some brief details about the performance metrics of VCO is also discussed. Chapter 3 gives detailed design implementation of VCO by dividing the design into number of small individual blocks such as LC tank, negative resistance, current source and buffers. Chapter 4 presents the simulation results of design double harmonic tuned (DHT) VCO compared to the normal LC tank VCO. Chapter 5 presents the conclusion and future work.
2 Oscillator theory

In this chapter, the basic classification of integrated oscillators and their tradeoffs such as noise and power are reviewed. Among the classifications the suited oscillator for GPS receiver is chosen. The major concern in this oscillator design for the GPS receiver is its noise, since the circuit and device noise can perturb both the amplitude and phase of output oscillation. So basic noise theories for good quality oscillator design is analyzed. The different performance metrics of oscillators like phase noise, tuning frequency range, figure of merit etc., are studied.

2.1. Barkhausen criteria

Oscillator is a system that converts the DC supply to an alternating current at a desired frequency. For a system to oscillate it should meet certain criteria called Barkhausen criteria [9]. Consider an unity-gain negative feedback system as in Figure 2.1. The closed-loop gain is given by,

\[
\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{H(s)}{1 + H(s)}
\]  

(2.1)

Where \( s = j \omega \), \( \omega \) is the angular frequency

If the system's open-loop transfer function \( H(s) \) at particular frequency \( \omega_0 \) becomes “-1”, then the closed-loop transfer function goes to infinite and the system becomes unstable. This unstable system might oscillate. There are two conditions for a negative-feedback system that should be satisfied for a system to oscillate,
In the above two criteria, the first one in equation (2.2) places a requirement on magnitude of the loop gain. In general, the magnitude is chosen to be two to three times larger than the required value to overcome the process and temperature variation. The second criterion in equation (2.3) shows for an oscillation to occur in a system, it should have an open loop phase shift of 180° or a closed loop phase shift of 360°. \( \angle H(j\omega_0) \) is the frequency-dependent phase shift.

### 2.2. Oscillator classifications

Generally oscillators are classified as harmonic oscillators and relaxation oscillators. For the design of VCO in chip, the integrated oscillator is used. By integrating the oscillator on chip, automatic calibration techniques become feasible and the benefits of integration makes the RF functions combined with other digital signal processing blocks. Further more, power consumption and area can be reduced. The mostly used integrated oscillators in recent days are of two types,

1. Ring oscillator
2. LC oscillator

The basic theory behind these two oscillators and their tradeoffs are discussed in the following sections.

#### 2.2.1. Ring oscillator

From the previous discussion on Barkhausen criteria, a system with open loop gain greater than one, which can be achieved by using an amplifier of higher gain. The second criterion is about having a phase shift of 180°, that can be done using inverting amplifiers. Simple common source (CS) amplifier acts like an inverter which has a maximum phase shift of 90°, that can be seen in the Figure 2.2. When the input at \( V_{in} \) is high, the transistor \( M_1 \) is on and all the current flows from \( V_{dd} \) to ground and so voltage at the output capacitor is low and when input is low, \( M_1 \) is off and the capacitor is charged to \( V_{dd} \). Thus, it acts like an inverter.

If the output of this CS amplifier is connected to the input, which acts like a negative feedback gives a phase shift of 180° and the inverter itself gives a frequency-dependent phase shift of 90° maximum which sums up to 270°. However this does not satisfy the second criteria on total phase shift around the loop and thus circuit does not oscillate. So the circuit with two stages of inverters are made and the output is connected to the input. Now the two stages gives a significant frequency-dependent phase shift of 180° but
the phase of output and input are same, so the circuit latches up and the circuit will not oscillate. So in order to have negative feedback an odd number of stages must be used, which gives 180° of phase shift and thus minimum of three stages should be cascaded to get a total of 360° phase shift. So, three or more stages need to be cascaded to get a ring oscillator and Figure 2.3 shows the block diagram of N-stage ring oscillator.

The frequency of ring oscillator depends on the number of stages and also the time delay of each stage. The frequency of oscillation is given by

\[
\text{Frequency} = \frac{1}{2\pi \sqrt{L C}} \times \left(1 - \frac{g_m}{g_m^*}\right)
\]
\[ f_{\text{osc}} = \frac{1}{2N} \frac{1}{t_p} \]  

(2.4)

Where \( f_{\text{osc}} \) is the oscillation frequency, \( N \) is the number of inverter stages, and \( t_p \) is the propagation delay of each stage.

For a ring oscillator with \( N \) identical inverter stages having a gain of \( A_0 \) and pole at \( \omega_0 \), the transfer function can be written as

\[
H(s) = \frac{-A_0^N}{(1 + \frac{s}{\omega_0})^N}
\]  

(2.5)

There are several advantages and disadvantages for ring oscillators. The major advantages are as follows, since the whole circuit is designed with transistors, it consumes very low chip area and the power consumption is very low. Different phase of output signals are easily achievable, and it has wide tuning range. The main drawback of ring oscillator is its poor performance in terms of phase noise. So ring oscillators are mostly used for clock generation in PLL, clock data recovery and in some clock synchronization applications rather than in RF transceivers where phase-noise becomes most important constraint.

### 2.2.2. LC oscillator

The LC oscillator has a LC tank in which inductor and capacitor are connected in parallel. The ring oscillator in the previous section is studied based on a feedback system. LC oscillator can be studied as a feedback system and also as one port oscillator. In this section, the LC oscillator is considered as one port oscillator and the phenomena of negative resistance is briefed. In ideal case if a LC tank is provided with a current impulse, the energy is transferred back and forth between the inductor and the capacitor producing oscillation for an infinite time period. However, this happens only when both the components are loss-less, i.e., if they have an infinite quality factor. In real case both have an resistance in them, which can be modeled as a parallel resistance \( R_p \) as shown in Figure 2.4, where the energy dissipates and thus the oscillation decays. To compensate the loss due to this resistance an active circuit is connected in parallel to the tank. This active circuit generates a negative resistance to cancel the parallel resistance \( R_p \), and thus it helps to sustain oscillation.

Integrated inductors have very low quality factor and consumes large area when compared to ring oscillator. Despite this factor, LC oscillators have proven to have very low phase noise compared to ring oscillator. Even with low quality factor the phase noise is reduced a lot compared to ring oscillator, still a major
research is carried out in increasing the quality factor of the inductor. Several different techniques are devised by studying the noise source in the oscillators. Details about the LC oscillator and a special technique called double harmonic tuning for reducing the noise in the oscillator is explained in the next chapter.

2.3. Noise sources in oscillator
In oscillators, major noise contributors are MOSFETS and inductors. There are two main sources of noise for MOSFETS: flicker (1/f) noise and the thermal noise [10],[11].

2.3.1. Flicker (1/f) noise
At low frequencies 1/f noise is a dominant noise source in MOSFET devices when compared to bipolar transistors. There are several theories that explain the presence of flicker noise in devices. One theory is the carrier number fluctuation theory which explains flicker noise as it occurs due to trapping and detrapping of charge carries in traps of gate dielectric. Flicker noise which is at lower frequency, due to up-conversion, affects the phase noise of the oscillator is explained in section (2.4.2. ).

2.3.2. Thermal noise
Thermal noise is another important noise source in an oscillator and due to the random movement of electrons in conductors by thermal agitation . This noise has a white spectrum, constant over frequency and is proportional to the absolute temperature. The spectral density of noise voltage and noise current of the
Oscillator theory

MOSFET is given by

\[ V_n^2(f) = 4kT \gamma \frac{1}{g_m} \]  \hspace{1cm} (2.6)
\[ I_n^2(f) = 4kT \gamma g_m \]  \hspace{1cm} (2.7)

Where \( k \) is the Boltzmann constant, \( T \) is the temperature in Kelvin, \( \gamma \) is the channel length modulation and \( g_m \) is the trans-conductance of MOSFET.

2.4. Noise theory

To make a low phase noise of oscillator one must know the theory behind the sources of noise in the oscillator. Two most discussed and important theories on phase noise are,

1. Leeson's proportionality
2. Rael's mixer base approach

These theories are discussed in the following sections.

2.4.1. Leeson's proportionality

Phase noise in LC oscillators is usually given by Leeson's proportionality [12]

\[ L(\omega_m) \propto \frac{1}{V_0^2} \frac{kT}{C} \frac{\omega_0}{Q} \frac{1}{\omega_m^2} \]  \hspace{1cm} (2.8)

Where \( L(\omega_m) \) is phase noise at \( \omega_m \), \( V_0 \) is oscillation amplitude, \( kT/C \) is Nyquist or thermal noise, \( Q \) quality factor of the inductor, \( \omega_0 \) is center frequency, \( \omega_m \) is frequency offset from the center frequency.

From equation (2.8) phase noise is given as \( kT/C \) noise shaped in the frequency domain by LC tank and normalized to the power of oscillation amplitude [13] and this is an empirical relation of phase noise by D.B. Leeson. Using this expression one could understand the factors affecting the phase noise of an oscillator. However to determine the noise contribution of each component to the phase noise of an oscillator, the above equation is insufficient. The proportionality is usually replaced by noise factor of the oscillator.

2.4.2. Rael's mixer based approach

In this approach Rael considered the oscillator as a mixer and then the noise factor is determined to estimate phase noise of the oscillator [14]. The noise factor \( F \) is calculated as total oscillator phase noise normalized to phase noise due to the resonator. Considering the oscillator in Figure 2.5, when both branches of the oscillator switches simultaneously, the tail MOS is pulled twice for each oscillation cycle. This makes the tail
Oscillator theory

node to oscillate twice the fundamental frequency and so the oscillator can be modeled as a single balanced mixer.

\[
F = 2 + \frac{8 \gamma R I_T}{\pi V_0} + \gamma \frac{8}{3} g_{mbias} R
\]  

(2.9)

The first term in equation (2.9) is from the inductor loss and second term is from negative resistance of cross coupled pair to compensate the inductor loss and the last term is from the channel length modulation of tail current source. By using this noise factor in Leeson's empirical formula, the phase noise of this topology can be estimated. The minimum noise that can be obtained from one topology is when considering the current source to be ideal and so neglecting the third term in equation (2.9), and also considering the differential pair as a pure current switch driving the resonator. And the voltage is given by,
Oscillator theory

\[ V_0 = \frac{4}{\pi} RI \] (2.10)

So by increasing current \( I \), \( V_0 \) can be increased and so from equation (2.8) noise can be reduced by \( V_0^2 \).

The amplitude is controlled by current in this region and is called “current limited regime”. Now substituting equation (2.10) and removing the third term in equation (2.9) minimum noise that can be obtained from the oscillator topology can be found.

\[ F_{\text{min}} = 2 + 2\gamma \] (2.11)

Where, \( F_{\text{min}} \) is minimum noise and \( \gamma \) is the channel length modulation.

Rael also in his paper [14] discusses about the noise conversion that happens in the oscillator. There are two main noise conversion happening in the mixer, first is flicker noise up conversion and second is second harmonic down conversion. In flicker noise up conversion, the low-frequency flicker noise mixes with the fundamental frequency and it resembles in amplitude modulated (AM) side bands and not a frequency modulated (FM) around the fundamental frequency. So this does not affect the phase noise, but the AM to FM conversion is carried out by high-gain varactors, and this can be reduced by reducing the gain of varactors but this in-turn reduces the tuning range of VCO. Second mechanism of conversion is the second harmonic down conversion. It is due to mixing action of oscillator. The tail node which oscillates at second harmonic mixes with the fundamental frequency, results in an up and down converted side bands. The up converted one lies far away from the fundamental frequency and so does not affect the phase noise. However, the down converted signal falls right into fundamental frequency and so affecting the phase noise adversely.

2.5. Oscillator parameters

Any electronic device has its performance parameters, which is universal to make it compare it with different topology of its kind. Similarly oscillator has few parameters and some important parameters are explained in the following section.

2.5.1. Center frequency

It is the fundamental frequency of the oscillator and is denoted by \( f_0 \). In the frequency spectrum, it is seen as a peak with most power. In our case, the center frequency is set to be at 1.5 GHz.

2.5.2. Tuning frequency range

It is the range of frequencies which the oscillator can generate. It is defined by the difference between
maximum frequency and minimum frequency.

2.5.3. Tuning voltage
It is the voltage that controls the capacitance of varactor to tune the oscillator for different frequency. The tuning voltage range also limits tuning frequency range, and this is defined by the charge pump in PLL.

2.5.4. Gain of VCO
It is the ratio of tuning frequency range with respect to minimum and maximum tuning voltage to the difference of tuning voltage, and it is denoted by kVCO with unit as Hz/V. Equation (2.12) gives the expression for the VCO gain.

\[
k_{\text{VCO}} = \frac{f_{\text{max}} - f_{\text{min}}}{V_{\text{tune, max}} - V_{\text{tune, min}}} \tag{2.12}
\]

2.5.5. Phase noise
This is one of the most important performance metrics of VCO, and it is the measure of power of frequencies around the fundamental frequency. The measurement is carried out in certain frequency offset from the center frequency for 1 Hz bandwidth, and it is measured in dBc/Hz.

2.5.6. Power dissipation
This is a measure of an amount of power used by the oscillator to oscillate. It is the product of supply voltage and tail current drawn from supply.

\[
P_{\text{diss}} = V_{dd}I_{\text{tail}} \tag{2.13}
\]

2.5.7. Figure of merit(FOM)
FOM is the widely accepted metrics to characterize and compare the performance of VCO with other VCO's. Show in equation (2.14) is the expression for calculating the FOM.

\[
FOM = L(\Delta \omega) - 20 \cdot \log \frac{\omega_0}{\Delta \omega} + 10 \cdot \log \frac{P_{\text{diss}}}{1\text{mW}} \tag{2.14}
\]

Where \(L(\Delta \omega)\) is the phase noise of oscillator at offset frequency \(\Delta \omega\) and \(P_{\text{diss}}\) is the power dissipation of the oscillator with center frequency \(\omega_0\).
2.5.8. **Figure of merit with tuning range (FOMₜ)**

Although FOM includes all important trade off parameters, tuning range is not included in it. Since tuning range also has greater importance in phase noise performance it is to be included in merit calculation. The equation (2.15) shows the expression for figure of merit calculation including tuning range.

\[
FOMₜ = L(\Delta \omega) - 20 \cdot \log\left(\frac{\omega_o}{\Delta \omega} \cdot \frac{FTR}{10}\right) + 10 \cdot \log\frac{P_{diss}}{1\text{mW}} \tag{2.15}
\]

Where \(FTR\) is the frequency tuning range.

2.6. **Oscillator in PLL**

To get a fixed frequency at the oscillator output, even with process variations, oscillator is placed in a PLL. Shown in Figure 2.6 is the block diagram of PLL which consists of a VCO, divider, phase frequency detector, charge pump and a loop filter. A reference oscillator usually a crystal oscillator with high accuracy is used in PLL to lock the VCO. The VCO's output is fed to a divider where the frequency gets divided to reference frequency. Then, PFD detects the phase difference between divided VCO output and reference oscillator.

And using the phase difference, charge pump along with loop filter produces tune voltage for the oscillator. Verilog model of PLL is made to study the function of the VCO in PLL. Verilog A code of different blocks of PLL can be found in Appendix A.
3 Voltage controlled oscillator design

The design of VCO becomes the top priority in the transceiver design as it is the most critical sub block of PLL circuit. It is an oscillating circuit whose output frequency changes in proportion to an input voltage. VCOs can be made to oscillate from a few Hertz to hundreds of GHz. In this chapter, different sub blocks of VCO are listed and design procedure for each sub block together with noise reduction techniques such as harmonic suppression, current mirror noise filtering techniques, are discussed briefly. S parameters simulation which is specifically used for LC tank design is also briefed. To give the output of VCO to different blocks of the receiver and not to load the LC tank directly, a buffer is used and its design is discussed.

3.1 Sub blocks of VCO

In general a VCO is considered as a black box with control voltage as input and an oscillating output as shown in Figure 3.1. The voltage of the output oscillation can be written mathematically as follow,

\[ V_{\text{out}}(t) = V_0 \cdot \sin(\omega_c t + \phi) \]  (3.1)

Where \( V_{\text{out}}(t) \) is the oscillation output, \( V_0 \) is the amplitude of oscillation, \( \omega_c \) is the angular frequency, and \( \phi \) is the phase of oscillation.

With the context of design procedure, VCO can be sub-divided into following blocks,

1. LC tank
2. Negative Resistance
3. Current Source
4. Buffer

These blocks are explained in the following sections.
3.2. LC tank

As discussed in the previous chapter about the negative resistance oscillator, the oscillation frequency is directly related to the LC tank. Shown in Figure 3.2 is the schematic of ideal LC tank. In real LC-VCO's the combination of inductor and varactors are used to get a variable frequency oscillator.

![Figure 3.2: Ideal LC tank](image)

LC tanks generally act like a bandpass filter and bandpass frequency is determined by resonant frequency of the tank, which is the frequency at which the reactance of the inductor ($X_L$) and capacitor ($X_C$) becomes equal.

Reactance of inductor ($L$)

\[ X_L = 2\pi f L \]  \hspace{1cm} (3.2)

Reactance of capacitor ($C$)

\[ X_C = \frac{1}{2\pi f C} \]  \hspace{1cm} (3.3)

At resonance,

\[ X_L = X_C \]  \hspace{1cm} (3.4)

Where $f$ is the frequency.

Substituting (3.2) and (3.3) in (3.4) the resonance frequency ($f_0$) can be determined,
Voltage controlled oscillator design

\[ f_0 = \frac{1}{2\pi \sqrt{LC}} \]  \hspace{1cm} (3.5)

Where, \( L \) and \( C \) are inductance and capacitance respectively.

Experimentally, this can be measured by running AC analysis on inductors and capacitors separately and plotting their reactance. As it is seen from the equations, inductive reactance should increase with frequency and the capacitive reactance should decrease with frequency. The point at which both curves intersect gives the resonance frequency as shown in Figure 3.3.

![Figure 3.3: Magnitude plot of inductive and capacitive reactances as a function of frequency](image)

The ideal LC tank discussed above is loss-less, but in real case there is an inherent resistance present with both inductor and varactor which can be determined by their quality factor (Q). Usually Q of an on-chip inductor is much smaller when compared to Q of varactor and so total Q of the tank is dominated by inductor's Q.

### 3.2.1. Scattering(S) parameters

The LC tank selected for final design in this work is a complex tank with two or more \( L \) and \( C \). S-parameter is a convenient way to analyze complex LC tank structures. The key idea used in s-parameter simulation is that a line terminated with characteristic impedance gives no reflection. The oscillator is considered as a two
port network and each port is terminated with an impedance of 50 Ω. There are four parameters for a two port network such as $S_{11}$, $S_{22}$, $S_{21}$ and $S_{12}$. The main parameter of our concern is $S_{11}$ input reflection coefficient, and it shows the tanks impedance at different frequencies.

Consider the normal LC tank in the Figure 3.4 which is terminated at both ends by a 50 ohm resistance. Port 1 is excited, and the reflection at port 1 is measured to get $S_{11}$. Figure 3.5 shows magnitude plot of $S_{11}$ against frequency. Values of inductor and capacitor used are 5 nH and 2 pF respectively, which corresponds to a frequency of 1.6 GHz approximately. In this plot magnitude '1' means the tank is open, and all the signal sent at that frequency is reflected back, and magnitude '0' means the tank acts like a short, and the signal is received completely at the port 2. The differential output seen across the terminals when there is short and open is zero and maximum respectively. The plot in Figure 3.5 shows it has an open at frequency around 1.6 GHz.
Voltage controlled oscillator design

GHz. These S-parameters do not give the exact figures on frequency of operation, and it discards potentially important informations regarding the process variations and parasitics. So this approach is used as start-up for determining the values of elements in the model with the expected behavior in hand.

3.2.2. Second harmonic suppression

Considering the Rael's mixer based approach on phase-noise theory discussed in previous chapter, as the oscillator's tail node oscillates at twice the frequency and main core oscillates at fundamental frequency, the oscillator can be modeled as a single balanced mixer. This second harmonic at tail node mixes with the fundamental frequency and gets down-converted as sidebands of the center frequency, which affects the phase noise. Even harmonics does not flow in the differential path as the oscillator is differential, but it flows through the tank. This in-turn affects the reactive balance between inductors and capacitors, and so is the frequency shift which influences phase noise of the oscillator. From this evidently the second harmonics is to be suppressed for a good VCO design.

There are several techniques to reduce second harmonics at tail node of the oscillator. Few of them are listed below,

1. Tail noise filtering technique
2. Third harmonic tuned tank
3. Second harmonic tuned tank
4. Double harmonic tuned tank

The first technique uses a filtering method by shorting second harmonics to ground. In remaining three techniques, tanks are designed such that they are self-immune to second harmonics, thereby reducing phase-noise of the oscillator. These three tank designs are briefed in the following sections with their reflection coefficient (S11) plot.

3.2.2.1 Third harmonic tuned tank

Shown in Figure 3.7 is the schematic of third harmonic tuned tank. The middle tank \( L_1 - C_v \) is tuned to fundamental frequency and the side tanks \( L_3 - C_3 \) are tuned to third harmonics. This combination gives nearly a short at second harmonic frequency. Main drawback of this design is the area, since the design uses three inductors, and also a LC filter has to be designed to provide a high impedance at the tail node for second harmonic attenuation. This again increases the number of inductors. So the technique of second harmonic tuned tank is used as discussed in next section.
Voltage controlled oscillator design

Figure 3.6: Magnitude of $S_{11}$ for third HT tank

Figure 3.7: Third harmonic tuned tank
3.2.2.2 Second harmonic tuned tank

In this design similar technique by suppressing second harmonics and allowing third harmonics is used. This is done by reducing the number of inductors and the design is shown in Figure 3.8. Main resonator tank \(L_1 - C_v\) is designed to fundamental frequency, and it provides open circuit at that frequency. The series \(L_2 - C_2\) combination is tuned to second harmonic frequency, and it acts as short to second harmonics. Here only two inductors are used and similar S-parameter plot is achieved. This suppresses second harmonics at tail node. The drawback of this tank is the short provided at second harmonic which is fixed and only fundamental frequency is tunable. This reduces second harmonic suppression over complete tuning range. To overcome this drawback a double harmonic tuned tank is introduced by slightly changing the tuning behavior of tank.

![Figure 3.8: Second harmonic tuned tank](image)

![Figure 3.9: Magnitude of S11 of second harmonic tuned tank](image)
3.2.2.3 **Double harmonic tuned tank**

The tank is designed in such a way that its fundamental frequency and second harmonic can be tuned by the varactor. The parallel combination of $L_1$ and $C_v$ forms the main resonator, and the series combination of $L_2$ and $C_v$ is tuned to second harmonic frequency, and this acts as a second harmonic short. Third combination of $L_2$ and $C_2$ acts as an open at third harmonic and Figure 3.10 shows the circuit diagram of the double harmonic tuned tank. Concept of the double harmonic tuned tank is discussed in [6].

![Figure 3.10: Double harmonic tuned tank](image)

![Figure 3.11: Magnitude of S11 of second harmonic tuned tank around second harmonics](image)
Voltage controlled oscillator design

Figure 3.12: Magnitude of S11 of double harmonic tuned tank around second harmonics

Figure 3.13: S-parameters' test setup
3.2.3. Design of double harmonic tuned tank

The design of DHT tank is selected as it has better performance over the other two types. This is because it suppresses the second harmonic throughout the tuning range. In this design, selection of L and C are challenging. The design can be carried out by sweeping the variables and determining the required response. However, this method is time consuming, hence a mathematical approach on such circuits is necessary. To determine the S-parameters mathematically, nodal analysis is carried out first on the test setup. Then by using equation solver tools (for example, Mathematica), the necessary parameter $S_{11}$ is determined.

Figure 3.13 shows the test setup for S-parameters of the DHT tank. A series resistance $R_1$, $R_2$ is added to the inductors $L_1$, $L_2$ respectively. Port-1 and Port-2 are terminated with 50 ohm resistance. Since the required parameter is $S_{11}$, a source at the input port is enough. Performing nodal analysis at nodes $V_1$, $V_2$, $V_3$ and $V_4$ the following equations are obtained,

$$\begin{align*}
\text{at node } V_1 & \quad V_1 = U_1 \\
\text{at node } V_2 & \quad \frac{(V_2 - V_1)}{R_s} + \frac{(V_2 - V_3)}{2} s C_v + \frac{(V_2 - V_4)}{R_2 + s L_2} + (V_2 - V_4) s C_1 = 0 \\
\text{at node } V_3 & \quad \frac{(V_3 - V_2)}{2} s C_v + \frac{(V_3 - V_4)}{R_1 + s L_1} = 0 \\
\text{at node } V_4 & \quad \frac{(V_4 - V_3)}{R_1 + s L_1} + \frac{(V_4 - V_2)}{R_2 + s L_2} + (V_4 - V_2) s C_1 + \frac{V_4}{R_s} = 0
\end{align*}$$

By solving these four equations the potential at each node can be determined.

To determine $S_{11}$, the load impedance at $V_2$ is to be determined. The load impedance is given by,

$$Z_L = \frac{V_2}{V_1 - V_2} R_s$$

where $Z_L$ is the load impedance, $V_1$ and $V_2$ are the node potential and $R_s$ is the source resistance.

The reflection coefficient ($\Gamma$) is given by,

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S}$$

where $Z_L$ is the load impedance given in equation (3.10) and $Z_S$ is source impedance (50 Ω).
After solving equation (3.11) and determining the reflection coefficient (\( \Gamma \)), a function called “manipulate” in mathematica is used to have interactive manipulation of values. So by entering the range of values of inductor and capacitor and also by specifying the frequency range, the plot can be obtained. This interactive plot helps in determining the values of L and C. The script for this is seen in appendix A.4. These calculated values are used as a starting point for observing the behavior of LC tank. The circuit can be fine tuned using real devices and S-parameters simulation in cadence tool.

3.3. **Negative resistance**

The designed tank in the previous section is lossy. It has an equivalent parallel resistance which can be determined by the quality factor of inductors and varactors. Usually in integrated circuit design quality factor of the tank is dominated by quality factor of the inductor. To compensate this loss and to sustain oscillations a parallel negative resistance equal to or greater than the tank resistance is added. Different topologies for designing parallel negative resistance is discussed in the following section.

3.3.1. **Topologies for cross coupled pair**

Cross coupled structures of PMOS, NMOS or both PMOS and NMOS can serve as a negative resistance and compensate the losses. Three different topologies are shown in the Figure 3.14. Three more variants of these topologies can be made by changing the position of tail source from top to bottom. Each topology has tradeoffs, and it lies in the designer’s hand to select the appropriate topology for the system. The NMOS only topology requires less area compared to the PMOS only topology because to generate the same transconductance the PMOS has to be twice or thrice the size of NMOS as the electron mobility is higher than the PMOS. The PMOS only topology has less flicker noise density compared to the NMOS only topology. The complementary topology has an advantage over PMOS only and NMOS only topology because the bias current is reused. The main drawback of this topology is the headroom availability, as minimum of three transistors has to be stacked and all the transistor to be in saturation with limited supply.
Figure 3.14: Three different negative resistance topologies with top (PMOS) current source
3.3.2. Design of cross coupled pair

For low-power performance, complementary MOS structure with PMOS current source is selected for generating the negative resistance. RF transistors from design library is used in the design. To do sizing of transistors, equivalent parallel resistance is to be calculated.

Quality factor of an inductor is given by,

\[ Q = \frac{R_p}{\omega_0 L} \]  

(3.12)

where \( R_p \) is the parallel resistance due to inductor quality factor, \( \omega_0 \) is resonance frequency of a tank and \( L \) is Inductance.

The condition for oscillator to sustain oscillation is,

\[ R_p = R_{\text{negative}} \]  

(3.13)

Consider Figure 3.15, impedance seen from the tank towards NMOS pair can be determined as follows,

\[ I_{in} = g_{m3} V_{gs3}, \quad -I_{in} = g_{m4} V_{gs4} \]  

(3.14)

Figure 3.15: Impedance seen from tank towards NMOS
Voltage controlled oscillator design

\[ V_{in} = V_{gs4} - V_{gs3} \]

(3.15)

Where \( g_m \) is the trans-conductance of MOS transistor and \( V_{gs} \) is the gate-source voltage of the transistor.

Combining equations (3.14) & (3.15),

\[ V_{in} = -\frac{I_{in}}{g_{m4}} + \frac{I_{in}}{g_{m3}} \]

(3.16)

The cross coupled transistors are equally sized and \( g_{m4} = g_{m3} = g_{m,n} \),

\[ R_{negative,nmos} = \frac{V_{in}}{I_{in}} = -\frac{2}{g_{m,n}} \]

(3.17)

Similarly, impedance seen from the tank towards PMOS side can be proven to be the same as in equation (3.17). And sizing both PMOS and NMOS such that all the transistors have the same trans-conductance so the total negative resistance is given by,

\[ R_{negative} = -\frac{4}{g_m} \]

(3.18)

From equation (3.13), the trans-conductance required to sustain oscillation is obtained. Then by using the general transistor current equation the initial value of the width and length of the transistors are determined. Generally, negative resistance is chosen two or three times larger than the required minimum to start up oscillation.

There is one more limitation on the sizing of the transistor in the complementary MOS topology which is the headroom. Since there is a need to stack two transistors for the cross coupled differential pair and two more on top for making a good current mirror, the design constraint on headroom is important. Design of current mirror increases in area as it operates close to the rail, and this is discussed in the next section. The cross coupled transistors are sized such that the total drop across the two transistor is 0.3 V less than \( V_{dd} \), that is giving 0.3 V design margin for the current mirror. The drop across each cross coupled transistors depends on its threshold voltage, which is defined by the technology. For general hand calculation, it is taken as 0.7 to 0.8 V. So the total drop across the two transistor is 1.4 to 1.6 V. Test setup is made, which is similar to the circuit in Figure 3.14(c), with a tail current source on top. The design is started with a current of 2 mA and the sizing is increased from the calculated value for required negative \( g_m \), to achieve margin of 0.25 V for the current mirror. Now to have a constant current source a current mirror with less than 0.25 V margin has to be designed.
3.4. **Current mirror**

The current source in Figure 3.14(c) should be replaced by a PMOS current source. The gate of the PMOS transistor should be controlled to get the required current, and it should be sized so that it lies in the saturation region. This can be achieved by making a current mirror circuit. Figure 3.16 shows the basic circuit of a current mirror. The transistor $M_2$ acts as a voltage controlled current source whose tail is fed to VCO. The current mirror copies the current from one branch to the other provided the transistors are sized properly to be in saturation region. From Figure 3.16 $I_{ref}$ is the reference current that is to be copied to $I_{tail}$. The current flowing through $M_1$ and $M_2$ can be written as

$$I_{ref} = \frac{1}{2} \mu_p c_{ox} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_{TH})^2$$  

$$I_{tail} = \frac{1}{2} \mu_p c_{ox} \left( \frac{W}{L} \right)_2 (V_{GS2} - V_{TH})^2$$  

Where $\mu_p c_{ox}$ is the process parameter, $W$ and $L$ are the width and length of the transistor.  

The ratio of these two currents can be given as

$$\frac{I_{tail}}{I_{ref}} = \left( \frac{W/L}{W/L} \right)$$  

$$\left( \frac{W/L}{W/L} \right)_1$$
Voltage controlled oscillator design

To have a better matching between the circuit the lengths of the transistors are sized equally. So the ratio becomes

\[
\frac{I_{\text{tail}}}{I_{\text{ref}}} = \frac{W_2}{W_1}
\] (3.22)

If \( W_2 = k \cdot W_1 \) then

\[
I_{\text{tail}} = k \cdot I_{\text{ref}}
\] (3.23)

Where \( k \) is the mirroring ratio

So from the previous design on negative resistance, the specification for current mirror is taken. The design specification made is listed in Table 3.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tail current</td>
<td>3</td>
<td>mA</td>
</tr>
<tr>
<td>Reference Current</td>
<td>200</td>
<td>μA</td>
</tr>
<tr>
<td>Voltage margin from ( V_{dd} )</td>
<td>0.25</td>
<td>V</td>
</tr>
<tr>
<td>Channel length minimum</td>
<td>2</td>
<td>μm</td>
</tr>
</tbody>
</table>

The reason for selecting minimum channel length as 2 μm is to avoid short channel effect and the noise is low for longer channel length.

3.4.1. Design

The condition for the transistor to be in saturation

\[
V_{ds} \geq V_{d\text{sat}}, \quad (V_{d\text{sat}} = V_{gs} - V_{th})
\] (3.24)

where \( V_{ds} \) is drain source voltage, \( V_{d\text{sat}} \) is saturation voltage, \( V_{gs} \) is gate source voltage and \( V_{th} \) is threshold voltage of the transistor.

The basic current equation of a PMOS transistor is given by

\[
I_d = \frac{1}{2} \mu_p c_{ov} \left( \frac{W}{L} \right) (V_{gs} - V_{th})^2
\] (3.25)
The current mirror is designed with transistor $M_1$ in the mirror branch as shown in Figure 3.16, whose size is to be determined. A current of 200 uA to is required to flow through it and also the transistor should be in saturation region. As $V_{dsat}$ should not be more than 0.25 V, for safer margin it is taken to be 0.2 V. Then by using the process parameters $(\mu_p, c_{ox})$ and a length of 2 um, the width of the transistor can be determined from the equation (3.25). Now by using the relation of current mirror from equation (3.22), the width of transistor $M_2$ can be determined, and thus the tail current will be mirrored the ratio times the reference current as in equation (3.23). The current mirror thus designed is tested in cadence spectre. The test is carried out by connecting a DC source at the tail node ($V_{tail}$), which acts as a load and then the potential is swept from 0 V to 1.8 V ($V_{dd}$).

The performance can be seen in Figure 3.17, where at around 1.6 V the current rapidly drops down, since the transistor $M_2$ is no more in saturation. This is to the design which has a margin of 0.2 V from $V_{dd}$. It can also be see that the tail current is not constant as the tail voltage increases towards $V_{dd}$. This is due to the impedance seen from the output node is low. To increase the impedance, cascode stages can be designed, but
Voltage controlled oscillator design

it has a problem of headroom. There are different topologies to implement cascode structures with low headroom and constant current. The most common topology is wide swing current mirror. However, in this VCO design a current mirror by Ivanov which has a high impedance is selected and used.

3.4.2. High impedance current mirror design

The high impedance current mirror by Ivanov [15]-[16] is similar to the basic current mirror with the cascode transistor and a differential amplifier as shown in Figure 3.18. The amplifier amplifies the potential difference between two nodes trying to maintain drain voltage of two transistors to be same, and it increases the impedance at the tail node. It allows the tail voltage to approach $V_{dd}$ even if the transistor $M_3$ enters the triode region. This property can be enhanced by increasing the gain of the amplifier. Shown in Figure 3.19 is an implementation of the amplifier by Ivanov using the transistors $M_4$ and $M_5$. By doing small signal analysis on the gain stage the gain can be determined to be

$$A = \frac{V_{out}}{V_x - V_y} = \frac{g_{md}}{g_{ds4}}$$  \hspace{1cm} (3.26)

$$g_{md} = \sqrt{2\frac{W}{L}} \mu_p C_{ox} I_D$$  \hspace{1cm} (3.27)

---

Figure 3.18: High impedance current mirror
Voltage controlled oscillator design

\[ g_{ds4} = \lambda I_D \]  

3.28)

\[
g_m4 \cdot g_{ds4} = \sqrt{2} \left( \frac{W}{L} \right) \mu_p C_{ox} I_D \cdot \frac{1}{\lambda I_D}
\]

(3.29)

From the equation (3.29) it is seen that the gain decreases with an increase in the drain current \( I_D \). Increases in channel length (\( L \)) keeping width (\( W \)) as constant decreases the \( g_{ds} \) and thereby increasing the gain. Sizing of the transistors \( M_1 \) and \( M_2 \) is carried out in the same method as in basic current mirror. For the cascode transistor \( M_3 \), the bulk connection is made to the drain instead of \( V_{dd} \) and with the width same as \( M_2 \) the length is made smaller to increase the impedance. The transistor is biased with a suitable DC voltage that makes the transistor \( M_2 \) to be in saturation, which can be implemented with basic current mirror stage. \( M_4 \) and \( M_5 \) transistor's widths are kept same as transistor \( M_1 \) and the length is reduced to
half, thus increasing the gain of the differential amplifier.

The circuit thus designed is simulated in cadence spectre with DC analysis by connecting the tail with DC source and sweeping the potential from 0 to $V_{dd}$. DC current through the transistor $M_3$ is plotted as shown in Figure 3.20. It also shows the comparison of the designed high impedance Ivanov current mirror and the basic current mirror. The tail node potential can reaches $V_{dd}$ by Ivanov's design with constant current.

### 3.4.3. Low noise current mirror

The current mirror designed above is noisy. The main sources of noise are the thermal noise and the flicker noise of the transistors and the noise from the reference current sources. Consider the reference current source $I_{ref}$ is mirrored by a factor of $N$, then the current at the output is given by,

$$ I_{out} = N I_{ref} \quad (3.30) $$

Similarly, the noise modeled as a current source is given by,

$$ I_{out,n}^2 = N^2 . I_{ref,n}^2 \quad (3.31) $$

So the noise at the output is square of the mirroring factor times the reference noise. As it is seen in the LC

---

**Figure 3.20:** Ivanov current mirror vs basic current mirror
Voltage controlled oscillator design

tank section, noise in the tail source gets converted to phase noise of the VCO by various phenomena, and this affects the performance of VCO. Considering VCO in context of PLL, the transfer function seen from VCO to output is like a high-pass filter. So low frequency noise in VCO is suppressed by the other block in PLL and only the high-frequency noise of VCO is seen at the output of PLL. This noise from the band-gap reference circuit and from the mirror branch can be suppressed by filtering technique. A typical low-pass filter as shown in Figure 3.21 can be employed for this purpose. The product of R and C will give the bandwidth of the filter, which should be less than the loop filter bandwidth of PLL. In this design, bandwidth for the filter is chosen to be 10 kHz. Since the poly resistors and MIM capacitors consume large area in the CMOS technology, a compromise should be made in sizing the devices. Moreover, resistance can be achieved by making the transistor work in triode region and using the on resistance, which will significantly reduce the area of the filter. Thus by choosing transistor as a capacitor and a resistor in the filter is designed. The resistance of the transistor in triode region is given by,

\[ r_{on} = \frac{1}{\mu_p C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)} \]  

(3.32)

Where \( r_{on} \) is the transistor resistance in triode region.

\[ \text{Figure 3.21: Bias noise filtering technique} \]
Voltage controlled oscillator design

There is one important drawback in this circuit, which is the start-up time of VCO due to time constant of RC filter. For the bandwidth of 10 kHz the start-up time is 100 us. This also decreases the locking time of the PLL. To overcome this a transistor $M_7$ acting like a switch is connected in parallel to the transistor $M_6$ in the RC filter as shown in Figure 3.22. By switching on the bypass transistor $M_7$, the capacitor in the filter can be charged faster than the required time constant, thus speeding up the start-up time of the VCO. Transient response of settling time of node Y with and without switch can be seen in Figure B.1.

![Figure 3.22: Bias noise filtering with speed up switch](image)
3.5. Buffers
Once the three components LC tank, negative resistance pair and the current source are designed the VCO can be tested for its performance. However, when it comes to system level, the VCO has to be connected to next block in the circuit. In a receiver, the VCO’s signal has to be fed back to PLL for locking the VCO to desired frequency and also to mixer to down-convert RF to IF. Directly connecting VCO’s oscillating output node to the next block will disturb the LC tank's behavior, as the next stage loads the tank. To isolate the tank from other components in the circuit a buffer has to be designed which does not load the tank. Shown in Figure 3.23 is the circuit diagram of buffer with single output stage. The main task of buffer is to distribute the VCO signal to different blocks as a differential current signal. This current is converted to voltage with low resistance and so the signal is immune to the parasitic capacitance in the distribution line. The number of differential output signals required depends on receiver architecture. In GPS receiver project a total of six output stages are required, as one for divider in PLL and remaining five for five mixers.

![Figure 3.23: Output buffer with single output stage](image_url)
3.5.1. Design of buffer

The capacitor \(C_1\) and \(C_2\) in the Figure 3.23 are used as decoupling capacitor to decouple the tank from the load. There is no DC at the output of the capacitor, so resistance \(R_3\) (\(R_4\)) along with the transistor \(M_6\) (\(M_8\)) is used to set the input DC level for the buffer. The combination of R and C acts as a high-pass filter. A 250 fF of RF metal-insulator-metal (MIM) capacitor is used for decoupling, due to its high-quality factor. The resistor \(R_3\) and \(R_4\) are selected to be 35 k\(\Omega\) forming 100 kHz high pass response, which is much lower than 1.5 GHz VCO center frequency.

The buffer designed in this circuit is a differential NMOS common source stage amplifier. The gain required for the differential common source stage is selected such that the buffer is sufficient enough to amplify minimum VCO amplitude obtained from the process variation simulation. The RF MOS transistors \(M_1\) and \(M_2\) are selected for the amplifier, as these transistors are modeled and optimized for high-frequency designs. The input DC voltage has to be set for leaving sufficient headroom to the current source (\(V_{dsat}\) of \(M_7\)). Using equation (3.33), current, size of transistor \(M_1\), and selecting required headroom for current source, gate voltage can be fixed.

\[
I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{g1} - V_{s1} - V_{th})^2
\]

(3.33)

Then output DC voltage (\(diffn\), \(diffp\)) can be set using equation (3.34).

\[
V_{diff} = V_{out} - I_{D1} R_L
\]

(3.34)

The output stage is a replica of the amplifier stage without the load resistor. Current output is thus taken and then can be used with a low-impedance load to make it immune to parasitic capacitance in the transmission line. Magnitude and phase response of designed buffer can be seen in Figure B.2.

3.6. Conclusion

In this chapter the various sub-blocks of VCO are analyzed and its design procedures are explained in detail. All designed sub-blocks are integrated to form a VCO, and this VCO has to be tested to analyze the noise performance and tuning frequency range.
4 Simulation results

In this chapter, discussion is made on different analysis techniques that are used to simulate and test the VCO. From previous chapter Different sub blocks of the VCO designed are integrated and tested for frequency and phase noise performance. To verify the theory of noise from tail current source in previous chapters, the oscillator noise is tested and measured with different current sources. To check if the designed VCO is suitable for GPS application, different simulations are carried out to check the change in frequency and phase-noise for different process corners, tuning range and also by varying supply voltage and current sources. The simulation results are plotted and conferred. The obtained results are compared with the different state of art architectures.

4.1 Analysis

Once the RF circuit is designed, depending on the requirement of the designer, there are several ways to analyze the design. Few analyzing techniques which are considered to be important for the design of VCO are discussed as follows,

- **DC analysis** or the large signal analysis, which is necessary to define the DC operating point of the circuit. This analysis is important in basic sizing of the transistors with some assumption on DC current through the devices. In this work it is used in all the sub blocks except the LC tank design.

- **AC analysis** or the small signal analysis, which is used in frequency simulation on circuits. In this work it is used in determining reactance and quality factor of inductor, capacitor and varactor, and also the resonance frequency of the tank.

- **Transient analysis** is used in determining the time-varying nature of the circuit. In this work, it is used to identify the start-up time of the current mirror and also for looking at the oscillation in the output node.

- **Scattering parameter analysis** or SP analysis is used in the design of complex LC tanks. In this work, the tank is considered as a black box and using sp analysis the input reflection coefficients are
determined.

- **PSS analysis** or the periodic steady state analysis is a RF extension of DC analysis. This analysis computes a steady-state response, and this state is used as a periodic operating point of the circuit for subsequent analysis. In this work for oscillators, it helps to predict the operating frequency, harmonics and their power.

- **Pnoise analysis** determines phase noise and considered to be one important characterization of the VCO. In this work it is ran on the steady-state solution obtained from the PSS analysis.

Usage of these analysis can be seen in the following sections.

### 4.2. Oscillator with ideal current source

Once the topologies of tank and negative resistances are selected and designed, with the help of theory from section (3.2.2.), the lowest possible noise can be determined. Referring to this, keeping the tail current source as ideal in the design, noise produced is minimum, which is contributed by inductor’s inherent resistance and by the negative resistance of differential pair. As shown in the Figure 4.1, an ideal current source from the analog library is chosen and the normal LC tank and DHT tank is tested for its phase noise performance using PSS and pnoise analysis. Shown in Table 4.1 is the comparison of performance between the two different tank topologies.

![Figure 4.1: Test setup for oscillator with ideal current source](image-url)
Simulation results

Table 4.1: Comparison of LC and DHT tank with ideal current source

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LC tank</th>
<th>DHT tank</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Tail Current (mA)</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset (dBc/Hz)</td>
<td>-130.4</td>
<td>-130.1</td>
</tr>
</tbody>
</table>

Note: The test was carried out with inductor quality factor of 10 and without varactors.

4.3. Oscillator with basic current mirror

In this test setup, ideal current source is replaced with basic current mirror from section (3.4.1.). Here, as the tail node of the oscillator is pulled twice for one oscillation cycle by the two branches, the tail node is expected to oscillate at twice the frequency of oscillation. The Figure 4.2 shows the plot of tail node voltage of LC tank and the DHT tank. As it is seen from the plot, DHT tanks partially attenuates the second harmonics at tail node. For the same power, DHT proves to give 5 dB less phase noise compared to normal LC tank.

Figure 4.2: Tail node voltage of oscillator with LC tank and DHT tank
Simulation results

Table 4.2: Comparison of LC and DHT tank with basic current mirror

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LC tank</th>
<th>DHT tank</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Tail Current (mA)</td>
<td>2.6</td>
<td>2.6</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset (dBc/Hz)</td>
<td>-115.7</td>
<td>-121.5</td>
</tr>
</tbody>
</table>

Note: The test was carried out with inductor quality factor of 10 and without varactors.

4.4. Oscillator with Ivanov's current mirror

In this test, basic current mirror is replaced by a high impedance current mirror (Ivanov current mirror) that was designed in section (3.4.2. ). The current mirror is designed to have a high impedance at its output, and in-turn creates a high impedance at tail node of the VCO. This can be seen in the Figure 4.3, where amplitude of the tail node is suppressed by Ivanov current mirror. A noise file is used for the reference current source in current mirror. Table 4.3 shows the comparison of LC and DHT tank. From results, it can be observed that noise from the reference branch is partially reduced by the DHT tank compared to the normal LC tank.

![Figure 4.3: Tail node voltage of DHT oscillator with basic and Ivanov current mirror](image-url)
Simulation results

Table 4.3: Comparison of LC and DHT tank with Ivanov mirror

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LC tank</th>
<th>DHT tank</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Tail Current (mA)</td>
<td>2.6</td>
<td>2.6</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset (dBc/Hz)</td>
<td>-117.6</td>
<td>-124.3</td>
</tr>
<tr>
<td>Noise % from reference mirror branch</td>
<td>83.7</td>
<td>65.5</td>
</tr>
</tbody>
</table>

Note: The test was carried out with inductor quality factor of 10 and without varactors.

4.5. Oscillator with noise filtering technique

Since the maximum noise contribution to oscillator's phase noise is from reference branch in the current mirror, noise filtering technique is adopted as in section (3.4.3.). Table 4.4 shows the comparison of the two tanks with tail noise filtering.

Table 4.4: Comparison of LC and DHT tank with noise filtering technique

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LC tank</th>
<th>DHT tank</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Tail Current (mA)</td>
<td>2.6</td>
<td>2.6</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset (dBc/Hz)</td>
<td>-124.6</td>
<td>-128.7</td>
</tr>
</tbody>
</table>

Note: The test was carried out with inductor quality factor of 10 and without varactors.

Now the test is repeated by replacing the ideal capacitors with varactors and MIM capacitors. Table 4.5 shows the comparison of both tanks after replacing the capacitors with varactors.

Table 4.5: Comparison of LC and DHT tank with varactors

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LC tank</th>
<th>DHT tank</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Tail Current (mA)</td>
<td>2.6</td>
<td>2.6</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset (dBc/Hz)</td>
<td>-123.1</td>
<td>-127.7</td>
</tr>
</tbody>
</table>

Note: The test was carried out with inductor quality factor of 10.

From the comparisons seen in previous section that the double harmonic tuning proves to have better phase noise performance over the normal LC tank with the same power specification.
4.6. **Frequency tuning curve**

To determine the gain of the VCO the tuning curve of VCO has to be determined. The test is carried out as in previous section with varactors. The tuning voltage is swept from 0.4 V to 1.4 V and Figure 4.4 shows the plot of frequency (blue) and phase noise (red) for different tune voltage.

![Figure 4.4: Oscillator tuning voltage against frequency and phase noise](image)

The gain of the VCO or $k_{VCO}$ calculated from the simulation is found to be 257 MHz/V. As seen in the plot of phase noise (red) for different tuning voltage, the measured phase noise at lower tuning voltage is low compared to higher tuning voltage. This is due to the quality factor of varactor, which is low at lower tuning voltage and it in-turn reduces the quality factor of the tank.

4.7. **Corner simulation**

Even with process variations, to determine if the VCO's tuning range is good enough for the PLL to lock at center frequency of 1.5 GHz, the VCO has to be tested with devices for different process corners. In this thesis work the corner simulation was carried out only for the core of the VCO which includes the negative resistance cross coupled pair and the tank. Hence, the main devices included for process corner simulation...
Simulation results

are RF MOS, varactor and RF MIM capacitor. A total of 27 corners and one nominal simulation are carried out. The plot of frequency for different corner cases are shown in Figure 4.5 for a tune voltage of 0.8 V. The lowest and highest frequencies obtained from the corner simulations are at 1.39 GHz and 1.556 GHz respectively.

To check if VCO lies well within the PLL locking range, the corner simulation is carried for lowest and highest tuning voltage of 0.4 V and 1.4 V respectively. Corner simulation plots for lower and higher Vtune can be seen in Figure B.3 and Figure B.4 respectively. The criterion is that frequency should be lower than 1.5 GHz at 0.4 V and greater than 1.5 GHz at 1.4 V. As seen in the figures, the VCO satisfies the criteria for 0.4 V for all the corners. However, at 1.4 V, three corners fall below 1.5 GHz and so the PLL would not lock at these corners. The lowest frequency is 1.489 GHz, which is 11 MHz below the center frequency. This can be adjusted by increasing either the tuning voltage or by increasing the size of the varactors.

![Figure 4.5: Corner simulation for VCO](image)
4.8. VCO performance on different bias points

The bias point in VCO plays a major role in frequency of oscillation, since the varactors are connected to the oscillation node. If there is a change in DC level of the output node, the varactors will be tuned and thereby changes the frequency. The DC bias point of the VCO mainly depends on the supply voltage and the tail current source. So, two tests are carried out to check the frequency performance of VCO, one by maintaining the constant current and sweeping the supply voltage and the second by keeping supply voltage constant and sweeping the current source.

4.8.1. Supply voltage vs frequency

Since the VCO designed is subjected to have limited headroom, the test was carried out for only small variation. The supply voltage ($V_{dd}$) is swept from 1.7 V to 2 V keeping reference source as constant at 200 uA and the plot in Figure 4.6 shows change in frequency for different supply voltages.

![Figure 4.6: VCO frequency for different supply voltages](image)
Simulation results

The frequency drastically drops at lower supply voltage due to the limited headroom and so DC level at output nodes are changed and so the varactors are tuned to different frequency. The constraint has to be put on Low Drop Out (LDO) regulator for having a regulated supply with a minimum of 1.8 V for using VCO with complementary MOS topology.

4.8.2. Reference current source vs frequency

Figure 4.7 Shows the plot of different frequencies by varying the current source and keeping the supply voltage constant at 1.8 V. The reference current source is swept for ±15 % of nominal current (200 uA), which is 170 uA to 230 uA.

![Figure 4.7: VCO frequency for different reference current source](image-url)
4.9. VCO performance over temperature

The test was carried out to check the performance of VCO for different temperature of operation. With constant supply voltage and current, and with a $V_{\text{tune}}$ of 0.8 V, the temperature was swept from -40 to 125 degrees C. The plot in Figure 4.8 shows the frequency and noise performance over temperature. Apparently phase noise increases with an increase in temperature, and this is due to thermal noise in the devices, and it is directly proportional to the temperature.

![Figure 4.8: Change of VCO frequency and phase noise over temperature](image)
4.10. Influence of varactor's quality factor in the tank

Second harmonic suppression is the key feature in both SHT and DHT tank, which helps in reducing the phase noise of VCO. In DHT structure, varactor plays a key role in suppressing the second harmonic for complete tuning range. Theoretically, suppression should be uniform for the complete tuning range. Here, due to the quality factor of varactor the suppression is not good and so the phase noise increases at lower tuning range, this can be seen from the red plot in Figure 4.9. However, if in SHT tank the second harmonic is fixed with high-quality capacitor and so the suppression is independent of the quality factor of varactor and this can be seen in the blue plot. Quality factor of varactor can be seen in Figure B.5.

![Figure 4.9: Phase noise of VCO with DHT and SHT tank for the tuning range](image)
## 4.11. State of art comparison

This section provides the comparison of designed architecture with state of art works, and it also presents the explanation for the difference in results of the presented work. Show in Table 4.6 gives the state of art comparison with the current work done and the description of each architecture is given in Table 4.7.

### Table 4.6: State of art comparison

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Process (nm)</th>
<th>Vdd (V)</th>
<th>Power consumption (mW)</th>
<th>Center frequency (GHz)</th>
<th>Phase-noise (dBc/Hz) @ 1 MHz offset</th>
<th>FOM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>130</td>
<td>1.2</td>
<td>0.35</td>
<td>3.2</td>
<td>-117</td>
<td>-191.6</td>
</tr>
<tr>
<td>[3]</td>
<td>350</td>
<td>2.4</td>
<td>6.72</td>
<td>2</td>
<td>-126</td>
<td>-186*</td>
</tr>
<tr>
<td>[4]</td>
<td>180</td>
<td>1.5</td>
<td>1.7</td>
<td>3.5</td>
<td>-122</td>
<td>-195.7</td>
</tr>
<tr>
<td>[5]</td>
<td>180</td>
<td>1</td>
<td>4.4</td>
<td>3.2</td>
<td>-133</td>
<td>-196.6</td>
</tr>
<tr>
<td>[6]</td>
<td>180</td>
<td>1.8</td>
<td>5.4</td>
<td>2.4</td>
<td>-137</td>
<td>-197.5</td>
</tr>
<tr>
<td>[7]</td>
<td>130</td>
<td>1</td>
<td>1.4</td>
<td>5.2</td>
<td>-131*</td>
<td>-194.5</td>
</tr>
<tr>
<td>[8]</td>
<td>180</td>
<td>1</td>
<td>4.6</td>
<td>2.5</td>
<td>-134</td>
<td>-195</td>
</tr>
<tr>
<td>DHT</td>
<td>150</td>
<td>1.8</td>
<td>5</td>
<td>1.5</td>
<td>-128</td>
<td>-185</td>
</tr>
</tbody>
</table>

* Phase noise @ 500 kHz offset
** Quadrature VCO

From the table above the figure of merit calculated for DHT VCO, and can be seen that it is higher than other state of art techniques. One main reason for the reduction in performance is that the reference current source, which is the main contributor of noise to the VCO, is neglected. The design of DHT is made based on two literatures [17] and [6], and there is a doubt that the power consumption determined for the calculation of FOM in both cases are not done properly. The reasons are as follows, considering [17] in the schematic of VCO the gate of the current source is connected to the current mirror's gate where a diode connection is missing, and so the gate connection of the PMOS transistor is floating. If this gate-gate connection is floating and if the potential is near to zero, the PMOS is on and maximum current flows through the transistor. Thus, VCO instead of working in current limited regime, works in a voltage limited regime and thus providing a square type of output waveform, which can be seen in the same. The DHT VCO designed in this project is
Simulation results
also tested with a floating gate-gate connection, and the plot of the output waveform can be seen in Figure B.6.

Table 4.7: Description of different architectures

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>Uses a technique of automatic amplitude calibration to compensate for process, voltage and temperature variation</td>
</tr>
<tr>
<td>[3]</td>
<td>Uses a noise-cancellation technique to cancel the tail current noise</td>
</tr>
<tr>
<td>[5]</td>
<td>Quadrature VCO with back-to-back series varactor configuration to minimize noise conversion</td>
</tr>
<tr>
<td>[6]</td>
<td>Double-harmonic-tuned tank to suppress the second harmonics generated at the tail node of VCO</td>
</tr>
<tr>
<td>[7]</td>
<td>Class C CMOS VCO which a type of differential Colpitts oscillator</td>
</tr>
<tr>
<td>[8]</td>
<td>All PMOS VCO which minimize flicker noise when compared to NMOS VCO</td>
</tr>
</tbody>
</table>

Similarly, in [6], gate of the tail transistor is controlled by external voltage. There is a possibility that the chip is measured with a lower gate voltage when compared to the designed VCO. This can be seen as the difference from the simulated and the measured results. Moreover the designed VCO in [6] is made to work with a center frequency of 2.53 GHz and a frequency shift can be noticed from the tuning curve of measured result. The phase noise measured at 2.53 GHz is very low when compared to the tabulated result in the literature. This same frequency shift is observed in the designed VCO when the gate voltage is lowered, the center frequency shifted from 1.5 GHz to 1.35 GHz with a current of 9 mA flowing through the tail transistor.
5 Conclusion

5.1. Summary

In this project, a study is carried out on the basics of an oscillator and its noise theory is reviewed. Literature survey on state of art architectures of the VCO are evaluated. Furthermore, the noise arising due to second harmonics at the tail node of an oscillator is discussed in detail. The ways to suppress inherently this second harmonic and thereby reducing the phase noise in the oscillator is also presented. A state of art work of double harmonic tuned oscillator with a good FOM and phase-noise performance is selected, and the design procedure is explained.

The double harmonic tuned VCO is designed for Galileo/GPS receiver with the help of 150 nm Lfoundry technology. The VCO operates with a center frequency of 1.5 GHz and has a power consumption of 5 mW. It has a nominal tuning range of 257 MHz for a 1 volt tuning voltage range. Phase noise measured at 1 MHz offset from the center frequency is -128 dBc/Hz. FOM calculated for the designed VCO is -185 dBc/Hz.

With the help of corner simulation, performance of the VCO is tested for tuning range and phase noise with different process corners on the components such as capacitors, varactors and RF transistors. Out of 27 corners and one nominal simulation, the VCO meets phase noise requirement in all corners but fails in three corners for tuning range.

The designed state of art architecture is compared with the performance of very basic LC tank cross coupled VCO. From the obtained results, evidently this built VCO has about 5 dBC/Hz less phase noise, which is a significant number. The design is also compared with the dual architecture of second harmonic tuned tank. The comparative results show its better performance than the double harmonic tuned tank. The reason of this behavior is due to the quality factor of varactor. The reasons for not achieving state of art FOM are also discussed.
Conclusion

5.2. Future work

The following points can be considered for future work:

- Second harmonic tuned tank gives lower phase noise when compared to the double harmonic tuned tank. But it is not optimized to the center frequency, so optimization can be done for the tank and so the phase noise can be reduced by 3 to 4 dB.

- Noise analysis on different VCO negative resistance topologies can be done before selecting any of the architecture as done in [14].

- The tuning range requirement is not full filled in few of the process corners. This issue can be taken care few different ways,

  1. The most common technique is the coarse tuning, in which an array of capacitors are used with switches to select between different tuning bandwidth, usually these switches for selecting different frequencies are taken externally and hardwired once the chip is made.

  2. Shifting the varactors tuning range. The center tuning voltage selected is not exactly at the center of varactors tuning curve. So by shifting the biasing of the varactor full tuning curve can be used.

  3. Redesigning the tank design by reducing the inductor size and increasing the varactor size can increase the tuning range, but this will increase the noise. So techniques like back to back varactors like in can be made to reduce noise conversion.

Study should be made in all three solutions mentioned above and select one of them to meet the tuning range requirement.

- Corner simulation with band-gap reference circuit is to be made to make sure if the VCO is suitable for manufacturing.

- Once all the above are met layout can be made for IC fabrication.
Bibliography


Appendix A

Verilog A code for different blocks like charge pump, divider and VCO are shown in the following sections. Mathematica script for determining coefficients of inductor and capacitor of the LC tank also can be seen.

A.1 Verilog A model for PFD and charge pump

`include "constants.vams"
`include "disciplines.vams"
module pll_pfd_cp(out, ref, fb);
output out; electrical out; // current output
input ref; voltage ref; // positive input (edge triggered)
input fb; voltage fb; // inverting input (edge triggered)
parameter real iout=100u; // maximum output current
parameter real vh=+1; // input voltage in high state
parameter real vl=-1; // input voltage in low state
parameter real vth=(vh+vl)/2; // threshold voltage at input
parameter integer dir=1 from [-1:1] exclude 0;
    // dir=1 for positive edge trigger
    // dir=-1 for negative edge trigger
parameter real tt=1n from (0:inf); // transition time of output signal
parameter real td=0 from [0:inf]; // average delay from input to output
parameter real rclamp=100 from (0:inf); // output clamp resistance
integer state;
analogue begin
    // Implement phase detector
    @(cross(V(ref)-vth, dir))
    if (state > -1) state = state - 1;
    @(cross(V(fb)-vth, dir))
    if (state < 1) state = state + 1;
Appendix A

// Implement charge pump
I(out) <+ transition(iout*state, td, tt);
// Implement output clamp (optional)
if (V(out) > vh)
    I(out) <+ (V(out) - vh)/rclamp;
else if (V(out) < vl)
    I(out) <+ (V(out) - vl)/rclamp;
// Add gmin to output to avoid convergence issues (optional)
I(out) <+ V(out)/1T;
end
endmodule

A.2 Verilog A model for divider

`include "constants.vams"
`include "disciplines.vams"
module pll_divider (out, in);
output out; voltage out;   // output
input in; voltage in;   // input (edge triggered)
parameter real vh=+1;   // output voltage in high state
parameter real vl=-1;   // output voltage in low state
parameter real vth=(vh+vl)/2; // threshold voltage at input
parameter integer ratio=2 from [2:inf);   // divide ratio
parameter integer dir=1 from [-1:1] exclude 0;
    // dir=1 for positive edge trigger
    // dir=-1 for negative edge trigger
parameter real tt=1n from (0:inf); // transition time of output signal
parameter real td=0 from [0:inf];   // average delay from input to output
integer count, n;
analog begin
    @(cross(V(in) - vth, dir)) begin
        count = count + 1; // count input transitions
        if (count >= ratio)
            count = 0;
        n = (2*count >= ratio);
        end
    V(out) <+ transition(n ? vh : vl, td, tt);
end
endmodule
A.3 Verilog A model for VCO

```verilog
`include "discipline.h"
`include "constants.h"
module vco(vin, vout);
  input vin;
  output vout;
  electrical vin, vout;
  parameter real amp = 1;
  parameter real center_freq = 1K;
  parameter real vco_gain = 1K;
  parameter integer steps_per_period = 32;
  real phase;
  real inst_freq;
  real resetph;
  analog begin
    inst_freq = center_freq + vco_gain * V(vin);
    $bound_step (1.0 / (steps_per_period*inst_freq));
    phase = idtmod(inst_freq,0,1);
    V(vout) <+ amp * sin (2 * `M_PI * phase);
  end
endmodule
```

A.4 Mathematica code to determine DHT tank's L and C

\[
Rs1 = \frac{(2\pi f L1)}{Q} \\
Rs2 = \frac{(2\pi f L2)}{Q} \\
Q \rightarrow 10
\]

Solve\{ V1 == U1, (V2-V1)G1+(sCv)/2 (V2-V3)+1/(sL2+Rs2) (V2-V4)+sC1 (V2-V4) == 0, \\
(V3-V2) (s Cv)/2+1/(sL1+Rs1) (V3-V4)== 0, V4 GS2 +(V4-V2)sC1 \\
(V4-V2)/(s L2 + Rs2)+(V4-V3)/(s L1 + Rs1) == 0\}, \{V1, V2, V3, V4\}

Zl = V2/(V1 - V2)/GS1 /. % // FullSimplify
s11 = (Zl - 50)/(Zl + 50)
Manipulate[
  Plot[Abs[s11 /. {Cv -> x1, L1 -> x2, L2 -> x3, C1 -> x4, GS1 -> 1/50, GS2 -> 1/50, U1 -> 1, U2 -> 0, Q -> 12} /. s -> -I*2*Pi*f],
    {f, 0.01*^9, 10.*^9}, PlotRange -> All, GridLines -> Automatic],
  Abs[s11 /. {Cv -> x1, L1 -> x2, L2 -> x3, C1 -> x4, GS1 -> 1/50, GS2->1/50, U1 -> 1, U2 -> 0, Q -> 12, f -> 1.5*^9} /. s -> -I*2*Pi*1.5*^9],
  Abs[s11 /. {Cv -> x1, L1 -> x2, L2 -> x3, C1 -> x4, GS1 -> 1/50, GS2->1/50, U1->1, U2 -> 0, Q -> 12, f -> 3.*^9} /. s->I*2*Pi*3.*^9],
  Abs[s11 /. {Cv -> x1, L1 -> x2, L2 -> x3, C1 -> x4, GS1 -> 1/50, GS2 -> 1/50, U1 -> 1, U2 -> 0, Q -> 12, f -> 4.5*^9} /. s -> -I*2*Pi*4.5*^9]],
  {{x1, 1.*^-12, "cv"}, 5.*^-13, 20.*^-13}, {{x2, 7.*^-9, "L1"}, 1.*^-9, 10.*^-9},
  {{x3, 5.423*^-9, "L2"}, 1.*^-9, 10.*^-9}, {{x4, 1.*^-12, "c1"}, 5.*^-13, 25.*^-13}]
Appendix B

Different plots that are used while designing and testing VCO is added in the following section.

B.1 Transient response of current source with filter

![Figure B.1: Noise filtering with and without start-up switch](image-url)
B.2 Magnitude and phase response of buffer

Figure B.2: Magnitude and phase plot of Buffer
B.3 Process corner for lowest tuning voltage

Figure B.3: Corner simulation with Vtune of 0.4 V
B.4 Process corner for highest tuning voltage

Figure B.4: Corner simulation with Vtune of 1.4 V
Appendix B

B.5 AC plot for quality factor of varactor

Figure B.5: Quality factor of a mos varactor

B.6 VCO output waveform with floating gate current source

Figure B.6: DHT VCO output waveform with floating gate connection