A New Mesochronous Clocking Scheme for Synchronization in System-on-Chip

Master thesis performed in Electronic Devices
By
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Linköping Institute of Technology

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All large-scale digital Integrated Circuits need an appropriate strategy for clocking and synchronization. In large-scale and high-speed System-on-Chip (SoC), the traditional “Globally Synchronous” (GS) approach is no longer viable, due to severe wire delays. Instead, new solutions such as “Globally Synchronous, Locally Asynchronous” (GALS) have been proposed. We propose to replace the GALS approach with a mesochronous clocking principle. In this work, such an approach together with a circuit solution in 0.18mm CMOS process has been presented. This solution allows clocking frequencies up to 4 GHz.
Abstract

All large-scale digital Integrated Circuits need an appropriate strategy for clocking and synchronization. In large-scale and high-speed System-on-Chips (SoC), the traditional “Globally Synchronous” (GS) approach is not longer viable, due to severe wire delays. In designs based on GS, clock skew becomes an important problem when the chip size increases. Instead new solutions as “Globally Synchronous, Locally Asynchronous” (GALS) approaches have been proposed. In this design style synchronous blocks are communicating with each other asynchronous. We propose to replace the GALS approach with a mesochronous clocking principle. The basic principle of this approach is communication of synchronous block using a master clock with unknown phase. In this work, such an approach together with a circuit solution in 0.18µm CMOS process has been presented. This solution allows clocking frequencies up to 4 GHz. The functionality of proposed scheme has been verified in three different steps. At first, the results of high-level simulation using VHDL are presented. Then transistor level of circuits is simulated using Cadence and finally post layout simulation has been done to make sure about the functionality of solution after actual implementation.
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1. Introduction

1.1. Basic Concepts

For very large-scale digital integrated circuits a clocking strategy is very important. Global synchronization (GS) is commonly used because designing based on GS is easy and well supported by CAD tools. One of the important drawbacks of a GS-based designed SoC is the relationship between physical size of chip and maximum clock frequency. Aside from this drawback, the clock skew in clock distribution networks becomes more serious when the chip size increases. Great attention and effort has been dedicated to skew and delay reduction techniques [1]-[3]. An H-tree implementation of a GS-based digital design is shown in Fig.1. In such a system a global clock must be delivered to all blocks at the same clock phase. It needs a symmetric layout style and limits design flexibility. To reduce clock skew in leaves it seems necessary to use wide metal wires in clock distribution network, which causes high power consumption in clock distribution. Some state-of-the-art designs of microprocessors show that 18-40 percent of power consumption is related to clock distribution network [4], [5]. In order to transfer data for long distance between two nonadjacent blocks, it is necessary to use short data transfers between adjacent blocks because long wires will have long delays. Consequently the total delay for data transfer increases and it results in clocking frequency and speed limitations.

According to these drawbacks another alternative for synchronization seems essential. To avoid problems related to GS-based designs, a method called asynchronous communication has been used [6]. In this style a global clock does not exist and all blocks are communicating via hand-shaking logic. However, this method of communication has not been popular because it is hard to design and to check the correct functionality. Also there is not a very high performance system to demonstrate the overwhelming advantages over the GS-based SoCs. To solve the mentioned problem related to globally synchronous systems, as another alternative, the
“Globally Synchronous, Locally Asynchronous” (GALS) design style has been introduced. In this method VLSI system is divided into smaller blocks each of which is using GS model. These blocks are communicating with each other using an asynchronous method. We propose to replace GALS with a mesochronous-clocking scheme [7], [8]. Fig.2 illustrates the idea behind this clocking strategy. In this strategy clock distribution is integrated in the buses (called strobe signal).

![Diagram of Global Synchronous Clocking](image1)

**Fig.1.** Global synchronous clocking

![Diagram of Mesochronous Clocking](image2)

**Fig.2.** Mesochronous clocking
As strobe signal is distributed along each link, it may be used for clock distribution for each of blocks. Therefore, obviously it can be assumed that the strobe at one of the incoming ports of each block can be used as local clock for that block. Then each of blocks may use its own clock or another clock coming from other blocks.

In this strategy, since there is no control on clock phases, having a specific control method to avoid failure in data detection like metastability problem seems necessary [9]. It means that transferred data should be retimed in such a way that incoming data to each of the blocks has an acceptable eye diagram. As the most important advantage of this clocking scheme, we should point out that data transfers for long distances may not limit clocking frequency because clock is transferred accompanying with data, resulting the same delay experience for data and clock signals. Therefore data transfer delay has no effect on clocking frequency and it is possible to increase frequency as much as single elements used for data retiming permit.

1.2. Purpose of the Thesis

In this work a new scheme for synchronization and clocking based on mesochronous clocking style, is proposed. To avoid data detection failures a proper solution seems necessary. The purpose of this thesis is introducing a new circuit solution to prevent any metastability failure in data detection.

All high level simulation has been done using VHDL. Also transistor level simulations and layout work has been done in 0.18 µm CMOS process using Cadence. A 1.8V power supply has been applied to circuit to reach a data rate of 4 GHz in data transfers.

1.3. Outline

In second chapter of the thesis, the failure related to unknown clock phase used in mesochronous clocking scheme is introduced. Also our proposed scheme is discussed and high-level models for different parts of circuit are shown. Third chapter is dedicated to explanation of our proposed scheme. In this chapter a high level perspective of scheme is discussed. In chapter 4
simulation results related to high level modeling of circuit is brought. In chapter 5 all circuits in transistor level implementation are shown. Chapter 6 shows the simulation results of transistor level scheme of circuit. In Chapter 7 layout of two sample blocks communicating with mesochronous method is shown. Chapter 8 is dedicated to post layout simulation results of proposed scheme. In final chapter conclusions about whole work is discussed.
2. Data Detection Failure

2.1. Introduction

As it was discussed in first chapter, in mesochronous clocking scheme we do not have any control on clock phase received by particular block. Each transmitter block sends strobe signal accompanying with data and after an unknown delay, receiver block receives strobe signal, which is translated as incoming clock. This clock is responsible for detection of incoming data, which is accompanied by strobe signal. At final step data should be aligned to the local clock of receiver block. Since incoming clock and local clock have an unknown difference in their phases, data detection by local clock may result in an unwanted failure. The metastability failure during data detection must be avoided by an appropriate solution. First of all, we want to look at the principle of metastability failure.

2.2. Metastability and Synchronization Failure

When sampling a changing data signal with a clock, the order of changing events between two signals determines the outcome. The smaller the time difference between events, the longer it takes to determine the outcome. When two events occur very close to each other, the decision time increases to more than expected time and a synchronization failure occurs \[10\]. To illustrate problem let us look at a NAND-latch in Fig.3. The latch is responsible for determining which of two signals $A$ or $B$ first rises. If one of these signals rises first, the corresponding output will go to low. Assume $A$ rises first and voltage difference between two outputs ($\Delta V$) tends to go high.
The upper NAND gate sinks a current of its output capacitance. $\Delta V_1$ is the changing of differential output voltage during the interval, $\Delta t$, from when $A$ rises to when $B$ rises:

$$\Delta V_1 = K \Delta t$$

(2.1)

K is a constant, which can be defined as ratio of current to capacitance of storage device, assuming constant current sinking during $\Delta t$ time interval. When $B$ rises the two NAND gates act as a cross-coupled sense amplifier that amplifies the differential voltage $\Delta V$ exponentially with time [10]:

$$\Delta V(t) = \Delta V_1 \exp(t/\tau_s)$$

(2.2)

Where $\tau_s$ is the regeneration time of the sense amplifier. From 2.1 and 2.2, the decision time, $t_d$, required for $\Delta V$ to attain unit voltage is given by

$$t_d = -\tau_s \log(K \Delta t)$$

(2.3)

According to 2.3 if two events occur very close to each other ($\Delta t \to 0$) the decision time, $t_d$, will be infinite. In such a situation circuit is in a metastable state. In this state a small change in $\Delta V$ will cause the output to converge to one of two truly stable states. In practice, noise causes that output converges to one direction. Certainly this state is an unwanted
situation in data detection process and it should be avoided by using a proper method.

2.3. Forbidden Zone

As it is discussed in section 2.2, to avoid data detection error caused by metastability, it is necessary to keep the clock edge using for data detection in a proper region. Assume that data is aligned to the rising edge of clock shown in Fig.4. When we want to read this data using another clock we need to define a forbidden zone in which data detection might suffer from metastability failure. It means that the clock edge used for data detection should be kept outside of this zone to make sure a safe data detection. This zone can be define as a time window with total length equal to the sum of the setup time and hold time of flip-flop used for data detection [11]. We can design a flip-flop in such a way that this window has a symmetric position around clock edge used for data detection. In this case we can simply define a symmetric forbidden zone as shown in Fig.4.

![Definition of forbidden zone](image_url)

**Fig.4. Definition of forbidden zone**
3. Proposed Scheme

3.1. Top Level of Scheme

In Fig. 5 the proposed synchronization scheme for one link between two blocks, is shown. Clk1 and clk2 are the local clocks in respective block. On the transmitter side, data is clocked by clk1 positive edge. In the same time the transmitter generates a strobe signal through a similar flip-flop, which clocked by clk1 negative edge. Since the strobe signal should have the same bandwidth as the data signal in order to have best delay matching between data wires and strobe wires this later latch is connected as a binary divider, so strobe signal changes at each negative clk1 edge. The data and strobe are transported in parallel along driver and bus, so they arrive with same delays to receiver side. This means that the strobe edges are aligned to the data eye also at the receiver.

Fig. 5. Proposed synchronization scheme
At the receiver side the strobe is converted to clk₁′ by a DLL-based frequency doubler. This is designed in such a way that each strobe edge gives rise to a rising clk₁′ edge. Clk₁′ is used to latch the incoming data which is delay matched with the frequency doubler (Δ delay). Then we need to retime this data aligned to clk₁′ to clk₂. This is done by latching the data clocked by clk₁′, by clk₂. Here we must choose the proper edge of clk₂, which does not coincide with the forbidden zone discussed above. This choice of using either clk₂ or inversion of that is performed by “Edge Decision” block shown in Fig.5. Since the DLL used for frequency doubling can generate different phases of incoming strobe signal, then the forbidden zone for edge decision is produced by the DLL. If the edge decision unit detects clk₂ positive edge in forbidden zone then the right edge for proper detection without metastability failure will be clk₂ negative edge. After proper data latching with one of the clk₂ edges data is aligned to the positive edge of clk₂ through the last flip-flop in the chain. The details of each part of circuits will be discussed in next subsection.

The expected waveforms at the receiving block are shown in Fig.6. In these waveforms it is assumed that the edge decision part has decided to select positive edge.

![Waveforms at receiving block](image-url)

**Fig.6. Waveforms at receiving block**
3.2. Elements of Scheme in System Level

In this section, two important elements, which have been used in proposed scheme, are discussed. These elements are “DLL-based frequency doubler” and “Edge decision unit” each of which consists of different circuits and a detail description of these circuits in gate-level and transistor-level is discussed in chapter 5. Here, only a system level description of blocks is presented.

3.2.1. DLL-Based Frequency Doubler

As mentioned in previous section, the frequency of clk₁ should become half, producing strobe signal because of having the same bandwidth for data and strobe. At receiving side we need to have a frequency doubler to get the same frequency as clk₁. This element can be reached by using a DLL. Proposed DLL is a digital DLL [12]. A block diagram of this digital DLL has been shown in Fig.7.

![Fig.7. Block diagram of digital DLL](image-url)
In such a digital DLL four different units can be considered. Input clock is applied to an inverter chain called “Delay Elements”. An Up/Down counter controls the load of each inverter in this chain and output of chain, in each clock cycle, is compared with input clock. The counter is clocked by output of a clock divider unit. “Clock Divider” unit divides the frequency of input clock by 4. The purpose of this division is to make sure about settlement of all circuits before each comparison between output clock and input clock. “Phase Detector” unit produces a signal to apply to “Up/Down” input of the counter. If counter counts up the load of inverters in chain increases and consequently the total delay of output clock is increases. If phase detector detects that input and output clock are matched, it produces a “Down” command to counter and it causes counter to count down to decrease the total delay. After lock, Up/Down output of Phase Detector will oscillate. Since after lock, DLL can produce different phases, the doubled frequency clock and also signal indicating forbidden zone discussed in section 2.3 can be reached by using XOR gates at the outputs of delay elements, as shown in Fig.8.

Fig.8. Frequency doubling using digital DLL
To have a better understanding about DLL-based frequency doubler, the related waveforms have been shown in Fig.9. The “Forbidden Zone” signal indicates a region around the rising edge of clk_1. It has been assumed that data is aligned to the positive edge of clock in transmitter block then it is necessary to keep the edge of sampling clock, which is used for data detection in receiver block, outside of forbidden region to avoid metastability failure.

![Waveforms related to DLL-based frequency doubler](image)

**Fig.9.** Waveforms related to DLL-based frequency doubler

### 3.2.2. Edge Decision Unit

The responsible unit for decision about proper edge of clk_2 (the local clock of receiver block) in order to be used for data detection, is “Edge Decision” unit. The structure of this unit has been shown in Fig.10. This
unit consists of two D-flip-flops and one multiplexer. At the beginning, the positive edge of clk₂ is selected by multiplexer. It means clk₂' is equal to clk₂. Then rising edge of clk₂' is compared with the signal indicating forbidden zone. If this edge is detected in forbidden area then the output of the first flip-flop rises and it causes a change in the output of second flip-flop. The output of second flip-flop acts as “select” input of multiplexer, and this change in out₂ causes multiplexer to flip the edge to negative one. Finally, clk₂' is used for detection of data which is aligned to clk₁' (the output of “Frequency Doubler” Unit) in receiver block, as illustrated in Fig.5. This decision guarantees that safe data detection without metastability problem can be done. Certainly it is essential to choose the forbidden zone in such a way that we keep the clock edge relatively far from the forbidden zone after a flip, in order to avoid multiple flips.

![Fig.10. Edge Decision Unit](image)

To illustrate the idea behind the “Edge Decision” unit, a set of related waveforms has been shown in Fig.11. When the positive edge of clk₂ is in forbidden zone then clk₂' is changed to the inversion of clk₂. It means the local clock of receiver block shifted by +180° when the rising edge is detected in failure zone. This shift keeps the clock edge used for data detection outside of problematic zone.
Fig. 11. Waveforms related to edge decision unit
4. High Level Simulation Results

In order to check functionality of proposed scheme the high level simulations by VHDL has been performed. In this simulation VHDL code for different components of scheme has been written and for different skews between clk2' and signal indicating forbidden zone, functionality has been checked. In Fig.12 waveforms related to “Edge Decision” unit is shown.

Fig.12. Waveforms related to Edge Decision Unit (Choice of falling edge)

According to Fig.12, at first, rising edge of clk2 is chosen by multiplexer as clk2’. When this edge is detected in forbidden zone flip-flops change their
outputs in such a way that the negative edge can be selected by multiplexer for \( \text{clk}_2' \). Out_1 and out_2 are outputs of flip-flops according to Fig.10.

Fig.13 shows the functionality of the same unit when the rising edge of \( \text{clk}_2 \) is not detected in failure zone. In this case outputs of flip-flops remain unchanged and the rising edge is applied to data detection in other parts of receiver block.

![Waveforms related to Edge Decision Unit (Choice of rising edge)](image)

**Fig.13. Waveforms related to Edge Decision Unit (Choice of rising edge)**

In Fig.14 waveforms related to data retiming in receiver part is shown. In this simulation a stream of bits, as incoming data, is applied to receiver block. The phase of \( \text{clk}_2 \) is changing slightly in such a way that after a while
the rising edge can be detected in failure zone. When the positive edge is detected in forbidden zone, the outputs of flip-flops (a and b) cause to change the clk₂’ to inversion of clk₂ and falling edge is chosen. Coming data is retimed by cascaded flip-flops according to Fig.5. Out₁–out₃ are respective outputs of flip-flops as it is shown in Fig.5. It is clear that out₂ is aligned to falling edge of clk₂ and out₃ is aligned to rising edge of that.

![Fig. 14. Retimed data in receiver block](image)

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5. Circuits in Transistor Level

5.1. Introduction

In this chapter, the circuits in transistor level have been presented. As it was discussed in Chapter 3, proposed scheme consists of different blocks each of which includes digital circuits. Here we are going to discuss about details of each of these circuits.

5.2. Basic gates

The basic elements of all circuits are digital gates. The schematic of these gates has been shown in Fig.15.

![Basic digital gates](image)

*Fig.15. Basic digital gates*
5.3. D-Flip Flop

D-flip flops are one of the important parts of transmitter and receiver blocks. This element is responsible for transmitting data and strobe from transmitter block and receiving and detection of data in receiver block. One of the high-speed and power efficient kinds of D-flip flops is “Transmission Gate Master-Slave (TGMS)” flip-flop. The structure of this flip-flop has been shown in Fig.16. In this circuit incoming data is sampled by falling edge of clock by transmission gate. In rising edge sampled data is transferred to the output. Feedbacks are applied to build a latch structure to avoid degradation of data.

![ TGMS D-Flip Flop and its Symbol ]
5.4. DLL-Based Frequency Doubler

As it was discussed in section 3.2.1, proposed digital DLL consists of four basic parts (see Fig.7). In this section circuits related to each of these parts are presented.

5.4.1. Delay Elements Unit

This unit is responsible for producing proper delay on incoming clock in order to shift it one period. This unit consists of 8 serial connected inverters with equal load. The amount of load at the output of each inverter is adjusted by feedback structure discussed in section 3.2.1. One of these inverters with its load has been shown in Fig.17. The inputs of transmission gates ($b_0$-$b_4$) are connected to outputs of 5-bit up/down counter. The bit $b_k$ ($0 < k \leq 4$) can add a load twice as much as load, which can be added by the bit $b_{k-1}$.

![Fig.17. One of inverters used in inverter chain with its load](image)

5.4.2. Phase Detector

This part is responsible for comparing the phase of the input clock with the phase of the clock coming out from output of last inverter in inverter chain. The structure of proposed phase detector is based on D-flip flop discussed in 5.3 with a slight difference. In order to reduce setup time of flip-flop to have a more accurate decision between two phases, the skewed
size has been used for first inverter and a delay has been introduce to clock signal of feedback part. The idea has been shown in Fig. 18. In this structure the first feedback is opened before sampling from delayed clock. It lets a faster data transfer from input of phase detector to middle storage node. The skewed inverter lets a faster level change from high to low in its output. Both of these mechanisms cause a shorter setup time for phase detector in order to have more accurate phase detection.

To be sure about the settlement of whole circuit before each phase comparison, a frequency divider is applied to decrease the frequency of incoming clock before applying to counter. This divider consists of two cascade D-flip flop each of which cause a division by 2. The outcome of this part has frequency 4 times less than that of incoming clock. The structure of this unit is illustrated in Fig. 19.

5.4.3. Frequency Divider

To be sure about the settlement of whole circuit before each phase comparison, a frequency divider is applied to decrease the frequency of incoming clock before applying to counter. This divider consists of two cascade D-flip flop each of which cause a division by 2. The outcome of this part has frequency 4 times less than that of incoming clock. The structure of this unit is illustrated in Fig. 19.

5.4.4. 5-Bit Up/Down Counter

As it was discussed in 5.4.1 a 5-bit up/down counter is responsible for changing the amount of load in the output of each delay element. The
outputs of this counter are connected to transmission switches, which can bring or remove capacitance loads in outputs of delay elements.

![Fig.19. Clock division by 4](image)

The counter receives its clock from output of clock divider shown in Fig.19. The up/down input of counter is connected to output of phase detector. After each phase comparison by phase detector, up or down command is produced and counter receives it. In every four clock cycle of coming clock to DLL counter decides to count up or down. A Schematic of counter has been shown in Fig.20.

### 5.5. Edge Decision Unit

The structure of this unit has been shown in Fig.10. This unit consists of two D-flip flops and one 2-input multiplexer. The circuit for D-flip flop has been already shown and the structure of proposed multiplexer is shown in Fig.21. If the “select” input has logic “1” the transmission gate with input “a” conducts and output becomes equal to the logic of input “a”. Otherwise the other switch is turned on and the logic of input “b” is conducted to the output of multiplexer.
Fig. 20. 5-bit up/down counter

Fig. 21. 2-Input Multiplexer
6. Transistor Level Simulation Results

After designing proper circuits for proposed scheme in transistor level, it is necessary to check the functionality in low-level design also. To do this, some simulations have been done using Cadence. All simulations have been done in 0.18\(\mu\)m CMOS process. In Fig. 22 the waveforms related to transmitter part are shown. Data stream and strobe signal are produced to send to another block. Since the frequency of strobe signal is half of the frequency of sampling clock in transmitter, the each edge of strobe is located in the middle of data eye.

![Waveforms related to transmitter](image)

**Fig.22.** Data and Strobe produced by transmitter

The waveforms related to our proposed digital DLL are shown in Fig.23. After “reset”, counter starts to count up because “up/down” input of counter is high (This input is produced by phase detector). When proper load is
applied to delay elements of DLL, input and output clocks have the same phase and DLL locks. The oscillation of Up/Down signal, produced by phase detector, shows that the DLL is locked.

![Digital DLL waveforms](image)

**Fig.23. Digital DLL waveforms**

Fig.24 illustrates the waveforms in “Edge Decision” unit. In this waveforms at first the positive edge of clk₂’ is detected inside of forbidden zone. Out₁ and out₂ are outputs of flip-flops of this block as shown in
Fig.10. These outputs flip in such a way that the $\text{clk}_2^*$ can switch into the falling edge of $\text{clk}_2$. This flipping causes that the proper edge is applied to data detection in receiving part.

![Graphs showing clock edge transitions](image)

**Fig.24.** Edge decision unit flips clock edge to the proper edge

Fig.25 illustrates the retiming process in receiving part for incoming data. After decision about appropriate edge for data detection, flip-flops at receiving blocks detect incoming data. The two retimed data aligned to $\text{clk}_1^*$ and $\text{clk}_2^*$ in receiving side are shown in this figure.
Fig. 25. Retimed data in receiving side by clk<sub>1</sub> and clk<sub>2</sub>
7. Layout

The last step of design is layout of two sample transmitter and receiver blocks. Layout of these blocks should be designed next to each other to have communication via metal wires. The layout task has been done in 0.18μm CMOS process. Transmitter consists of two flip-flops and some inverters and drivers. The main part of layout is dedicated to receiver block. Fig.26 shows layout for 5-bit counter used inside of digital DLL.

![Fig.26. Layout of 5-bit up/down counter](image-url)
In proposed digital DLL, an inverter chain with their load has been used. We called in “Delay Elements”. Layout for this unit has been shown in Fig.27.

![Fig.27. Layout of delay elements](image)

Finally, whole parts of blocks consisting of digital DLL, delay elements, flip-flops, multiplexers, digital gates and clock drivers are connected together in different parts of layout to build whole layout. The layout of whole circuits consisting of two sample transmitter and receiver blocks has been shown in Fig.28. The size of active area is 260µm × 80µm.
The last step of verification is post layout simulations. In next chapter the results of post layout simulations are brought.
8. **Post Layout Simulations**

After completing layout of two sample blocks, post layout simulation must be done to be sure about functionality after adding parasitic elements to circuit. This parasitic elements can degrade performance of circuits in some parts then it seems necessary to check functionality and performance after layout also.

In Fig.29 the post layout simulation for digital DLL at 70° C temperature and 1.5 GHz input clock has been shown.

Fig.29. Digital DLL at 70° C and 1.5 GHz input clock after layout

Fig.30 shows the post layout simulation related to “Edge Decision” unit.
In this simulation, $clk_2'$ (the output of “Edge Decision” unit) switches to inversion of $clk_2$ (the local clock of receiver block) when the rising edge of $clk_2$ is detected in failure zone. $Out_1$ and $out_2$ are outputs of flip-flops according to Fig.10.

![Post layout simulation for “Edge Decision” unit](image)

**Fig.30.** Post layout simulation for “Edge Decision” unit

In Fig.31 the results related to data retiming in receiver blocks has been shown. Incoming data to receiver block is detected by $clk_1'$ (the output of frequency doubler unit). After appropriate decision by “Edge Decision” unit about the proper edge of $clk_2$ (the local clock of receiver block) $clk_2'$ has been produced and data is aligned to its rising edge.

In this simulation the $clk_2'$ is the inversion of $clk_2$ then in second step data is aligned to the falling edge of $clk_2$. At last step data is retimed by rising edge of $clk_2$. 
Fig. 31. Incoming data is retimed in receiver block
9. Conclusions

A scheme based on mesochronous clocking for synchronization in System-on-Chip and a circuit solution to avoid the metastability failure has been presented. All related circuits in system level and in transistor level has been discussed. To check the functionality of proposed scheme, high-level simulations using VHDL are presented. Also to check the functionality and performance of scheme transistor level simulations are done by Cadence. Layout task of two sample block and post layout simulations are the final part of thesis research to be sure of real performance of circuits after fabrication. According to the results obtained, in this solution by using 0.18µm CMOS process, it is possible to increase clocking frequency up to 4 GHz. In this case, data rate can also increase up to 4 GHz. It allows us to run the circuit with a high-speed data transmission between different blocks in a proposed SoC.
References


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